APPLICATION NOTE

Improved Picture Quality Module MK6-V1 V2.0

AN97017

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Abstract

This document describes the hardware content, the signal processing and the software control of the 100 Hz scan converter module MK6. The module can be implemented into different TV signal processing architectures. This means, it can be adapted to different colour decoder and deflection processor concepts.
The main signal processing features of the module are 100 Hz scan conversion with median filter based line-flicker reduction, progressive scan, vertical zoom, noise reduction and cross colour reduction. These features are provided by the SAA 4990 (PROZONIC). Also a horizontal aspect ratio conversion can be performed, either by the optional IC SAA 4995 (PANIC), or by an appropriate frequency ratio of the memory writing to the reading frequency, if the IC SAA 4995 should not be used.
The memory controller SAA 4952 is applied to generate the necessary clock and control signals for the memories and the signal processing ICs. This module is also equipped with a slave microcontroller which provides an easy to handle external I²C user interface and controls internally the above mentioned signal processing ICs via the SNERT-bus interface.
The I²C bus user interface is described in detail in this document.

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Keywords

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LFR
MOVIE PHASE DETECTION
PROGRESSIVE SCAN

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Summary

The IPQ-Module is a scan converter with analog baseband inputs and outputs Y,-(R-Y) and -(B-Y). It supports the following display modes:

- 50/60 Hz to 100/120 Hz conversion with line flicker reduction LFR (AA*B*B) or a simple field repetition (AABB)
- Progressive Scan 50 Hz/1250 lines or 60Hz/1050 lines, interlaced
- Frame repetition mode for movie sources
- Multi-PIP support
- Horizontal zoom (10%, 12.5%, 33%, 50% or 100%)
- Horizontal compression linear and nonlinear with 33%
- Advanced still picture (AA*AA*)
- Vertical zoom (10%, 12.7%, 33%, 50% or 100%)

Additionally the following main features are supported:

- Digital CTI (colour transient improvement)
- Luminance peaking function
- Adaptive noise and cross-colour reduction with different reduction levels
- Black side panels
- Screen fade
- Adaptive LFR control for movie sources

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1. Introduction

1.1 Definitions, Acronyms and Abbreviations

IPQ µC	Improved Picture Quality slave microcontroller
HEX	Hexadecimal program file
ECO4	Economy Controller IC 4
SNERT	Synchronous No parity Eight bit Reception and Transmission
PANIC	Panorama IC
PROZONIC	Progressive Scan Zoom and Noise Reduction IC
VEDA	Video Enhancement Digital to Analog Converter
VDFL	Vertical deflection pulse
HDFL	Horizontal deflection pulse
FRS	Functional Requirements Spec

1.2 References

[1] SCP Philips Semiconductors Software Creation Process, Wilko van Asseldonk, Marc De Smet, 9.4.96, V1.0

[2] The IIC-bus and how to use it, 12 NC-No.: 9398 393 40011

[3] SNERT bus specification see application note AN95127

[4] S87C654 (µC) data sheet, Philips Semiconductors

[5] TDA 8755 (ADC) data sheet, Philips Semiconductors

[6] SAA 4952 (ECO4) data sheet, Philips Semiconductors

[7] SAA 7165 (VEDA) data sheet, Philips Semiconductors

[8] SAA 4995 (PANIC) data sheet, Philips Semiconductors

[9] SAA 4990 (PROZONIC) data sheet, Philips Semiconductors

[10] TMS 4C2970 (field memory) data sheet, Texas Instruments

[11] TDA 9151, TDA 9152 (Deflection processor) data sheet, Philips Semiconductors

[12] Data Handbook, Fast TTL Logic Series, IC 15, Philips Semiconductors

[13] Data Handbook, High-speed CMOS logic family, IC 6, Philips Semiconductors

[14] PAL plus Decoding using SAA4996 and SAA4997, Application note AN95126, Philips Semiconductors

2. Hardware description

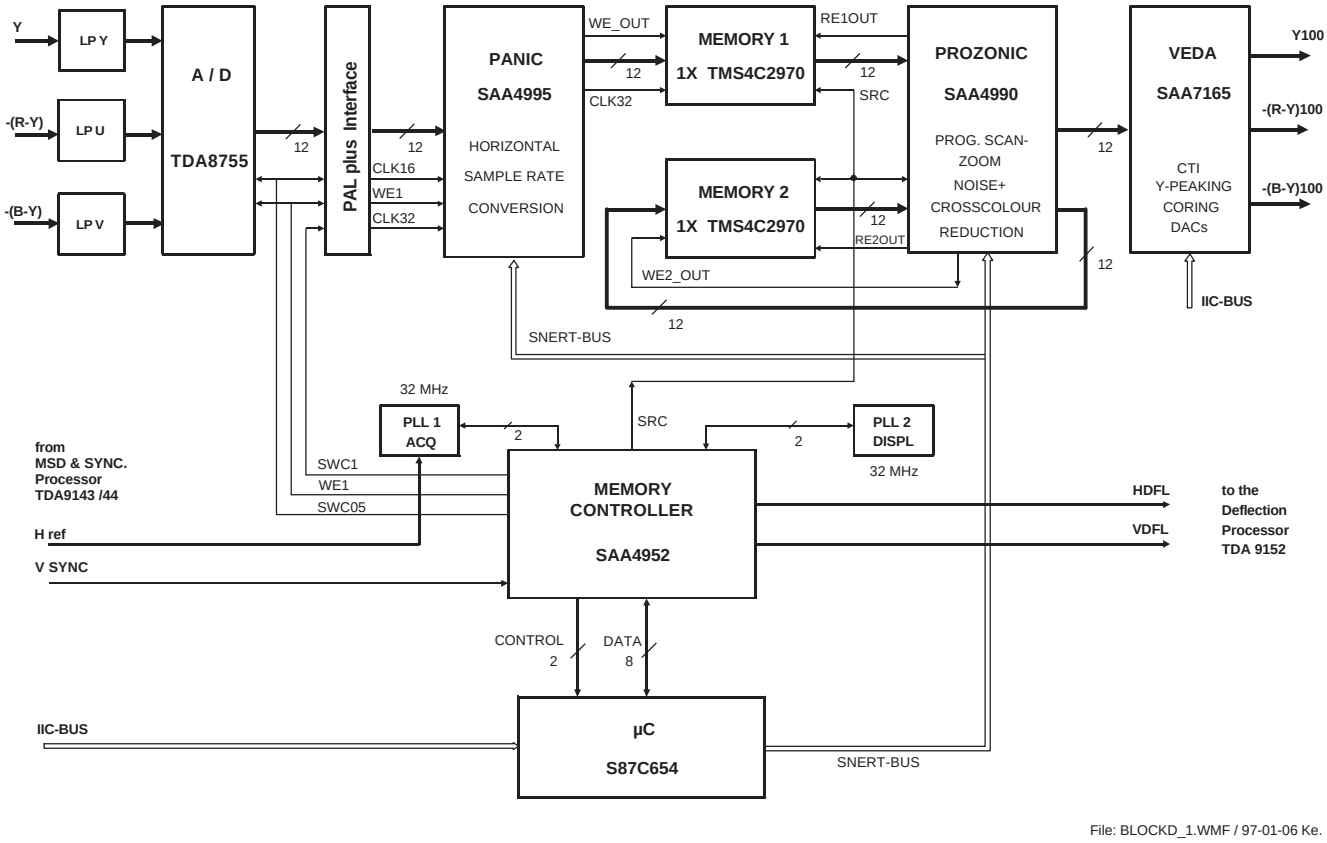

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Fig.1 Blockdiagram of the IPQ Module with PANIC

The MK6V1 module is prepared to support different system configurations. Always two field memories are implemented. The video data is written into memory 1 [9] and read twice. At the output of memory 1 the field frequency is doubled to 100 / 120 Hz. The data is fed via the progressive scan, zoom and noise reduction IC PROZONIC [9] to the video enhancement and DA converter VEDA [7]. The VEDA IC performs an upconversion of the data rate from 4:1:1 (or 4:2:2) to 4:4:4 before the DA conversion is done. Furthermore a digital colour transient improvement, a luminance peaking and a coring function can be activated via I²C bus by the user.
For a simple field repetition mode the data can be reconverted to analog output signals without additional processing in front of the SAA 7165. If the line flicker reduction (LFR), progressive scan or zoom feature is active the information is written into field memory 2 [9]. This memory works as a 50 / 60 Hz field delay. By the help of this second field memory PROZONIC is able to process information of a whole frame, e.g. PROZONIC

a) calculates the median filtered fields A* and B* in the sequence AA*B*B for field rate upconversion with LFR,
b) calculates the median filtered lines odd and even for progressive scan conversion,
c) averages between incoming and previous fields for the adaptive noise and cross-colour reduction obtained by a recursive filter in the 2 fh domain and
d) interpolates lines for the vertical zoom function or progressive scan.

If a scan converter is used along with an analog colour decoder frontend an AD-Converter is necessary to convert the three baseband input signals Y, -(R-Y) and -(B-Y). Those signals are preamplified and low pass filtered to avoid antialiasing effects.
The 8 bit triple AD-Converter TDA8755 [5], applied in this IPQ module, has an integrated clamping function and is equipped with a data formatter. The data formatter converts the signal data provided by the AD conversion into a 12 bit data format, 8 bit for luminance and 4 bit for the serial chrominance output data format (bandwidth ratio Y:U:V = 4:1:1). These data are supplied to the digital data output bus of 12 bits width.

The SAA 4995 (PANorama IC) is an add-on device to be used between AD-Converter and the first field memory. It performs:

a) a linear horizontal sample rate conversion with the capability to zoom and compress the picture with a conversion rate between 0.5 and 2,
b) a dynamic sample rate conversion for a panorama display of e.g. 4:3 picture material on a 16:9 display without side panels.

In panorama mode the sample rate conversion factor is modulated along the video line. For the panorama function the picture is compressed in horizontal direction in the middle of the screen and zoomed at the sides. It is also possible to program the inverted function. The PANIC has to be supplied with 16 MHz and also the double frequency of 32 MHz which is used for the sample rate conversion filter. The field memory 1 is supplied with a writing clock of 32 MHz. The WEout of PANIC determines when a pixel shall be written. In a normal mode without compression or zoom the logical status of the WE signal will change from clock to clock. If a zoom factor of two is active the WE signal will remain in the logical high status for the whole active line.

The acquisition PLL generates the 32 MHz writing clock. The display PLL which is intended to have a large time constant and a small tracking range (+/- 6 %) is generating the 32 MHz display clock. A double clock system has advantages if an unstable source like a VCR is connected to a 100 Hz converter.

All control signals to run the module and reference signals for the PLLs are generated by the SAA 4952 [6]. The memory controller itself is controlled by a microcontroller S87C654 or S87C652 via an 8 bit parallel interface [4]. Every vertical blanking period of the display is used to transmit the desired register settings to the SAA4952 dependent on the chosen mode of the module. Additionally the microcontroller communicates via a three wire SNERT bus interface [3] with the PANIC and PROZONIC.

Besides the 100 Hz / 120 Hz conversion it is also possible to run a progressive scan mode. In this case the reading of the memories is changed to 50 / 60 Hz field frequency. The inserted lines are generated by median processing in the PROZONIC IC. Also this conversion mode can be combined with the vertical zoom function and in contrast to the 100 Hz mode it is also possible to realize a vertical compression.

The synchronization of the module is obtained by providing a vertical synchronization signal 50 / 60 Hz and a horizontal synchronization signal 15.625 / 15.750 kHz. The latter can e.g. consist of clamping pulses or line blanking pulses. The software can adapt the internal field recognition in the memory controller to any synchronization pulse (H to V) timing condition.

The various modes of the IPQ module are activated via a simple IIC-Interface [2] of the microcontroller on the board.

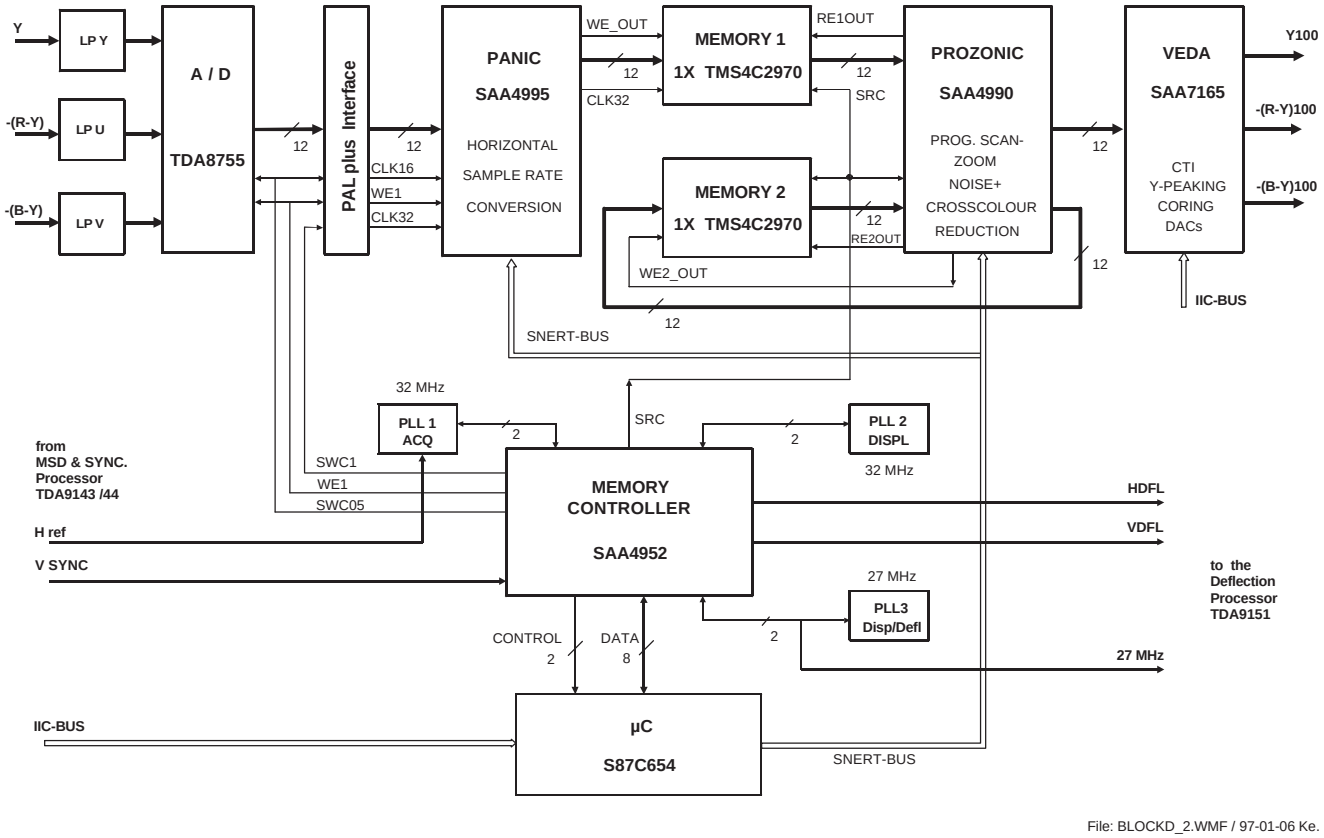

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Fig.2 Blockdiagram of the IPQ Module containing PANIC and an additional display PLL to drive the Deflection Processor TDA9151.

The IPQ application of Figure 2 assumes that a TDA 9151 is used as Deflection Processor. This device needs a 27MHz linelocked clock signal. Compared to the system explained before an additional 27 MHz PLL has to be implemented. The 32 MHz display PLL is locked to the horizontal deflection pulse HDFL from the memory controller. The 27 MHz deflection PLL is coupled to the externally provided Href signal. The tracking range and the bandwidth of this PLL has been restricted to ensure a good jitter (high frequent time base distortions) suppression. Thus a stable linelocked clock signal generation is given even at Href signals with a poor time base stability. The 32 MHz display PLL is coupled to the horizontal deflection pulse HDFL. Its tracking range and bandwidth is larger compared with the deflection PLL to achieve a fast and perfect synchronization between the deflection and the display data read from the memories.

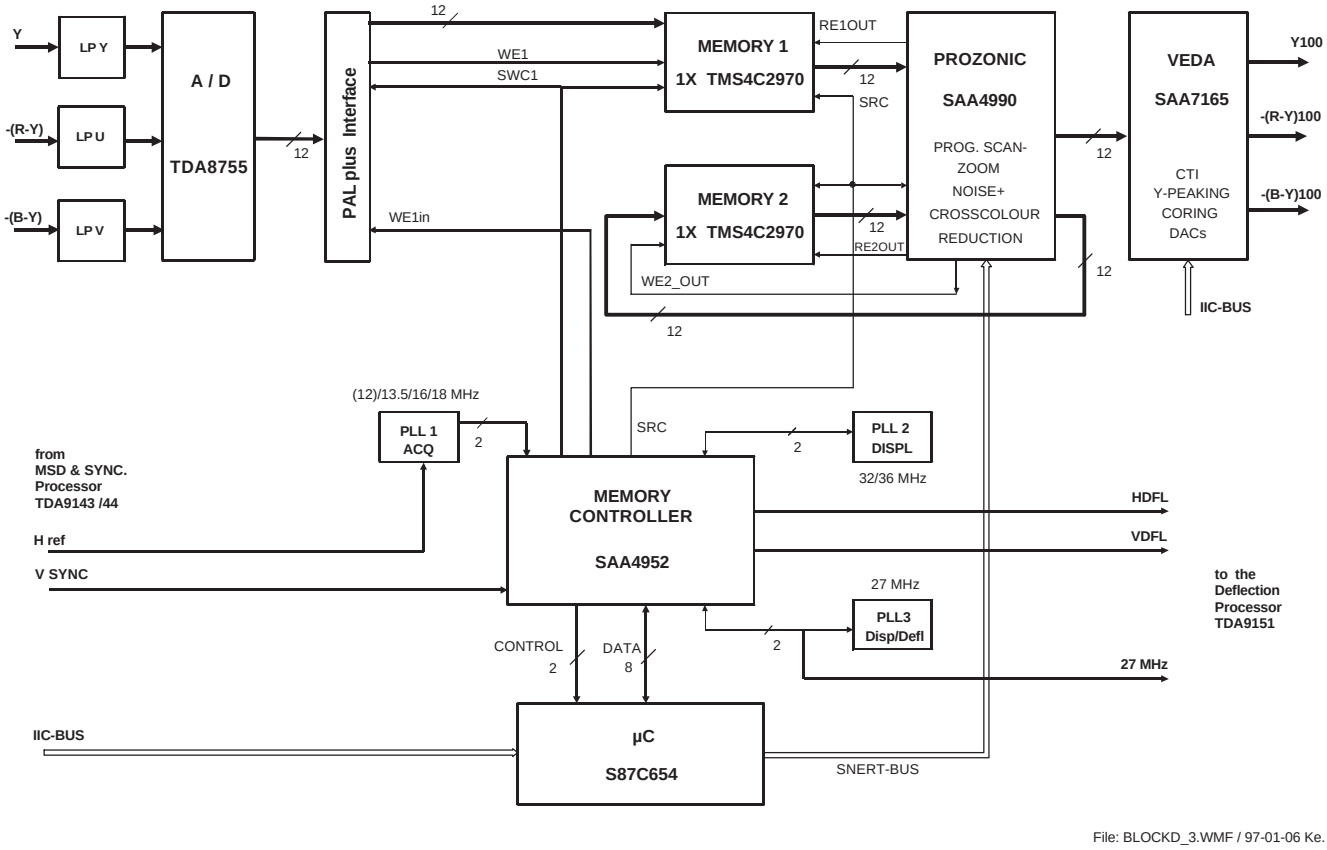

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Fig.3 Blockdiagram of the IPQ Module without PANIC, containing a additional Display PLL to drive the Deflection Processor TDA9151.

The IPQ application in figure 3 does not include the SAA 4995 (PANIC). The different horizontal zoom and compression ratios are realized by the combinations of writing to reading frequency of the memories. The acquisition PLL can generate the following frequencies: (12), 13.5, 16 and 18 MHz. This PLL uses a VCO whose frequency is switched to the desired frequency. As display frequencies 27, 32 and 36 MHz are supported. The PLL2 is not switched. It is able to generate 32 MHz as well as 36 MHz.

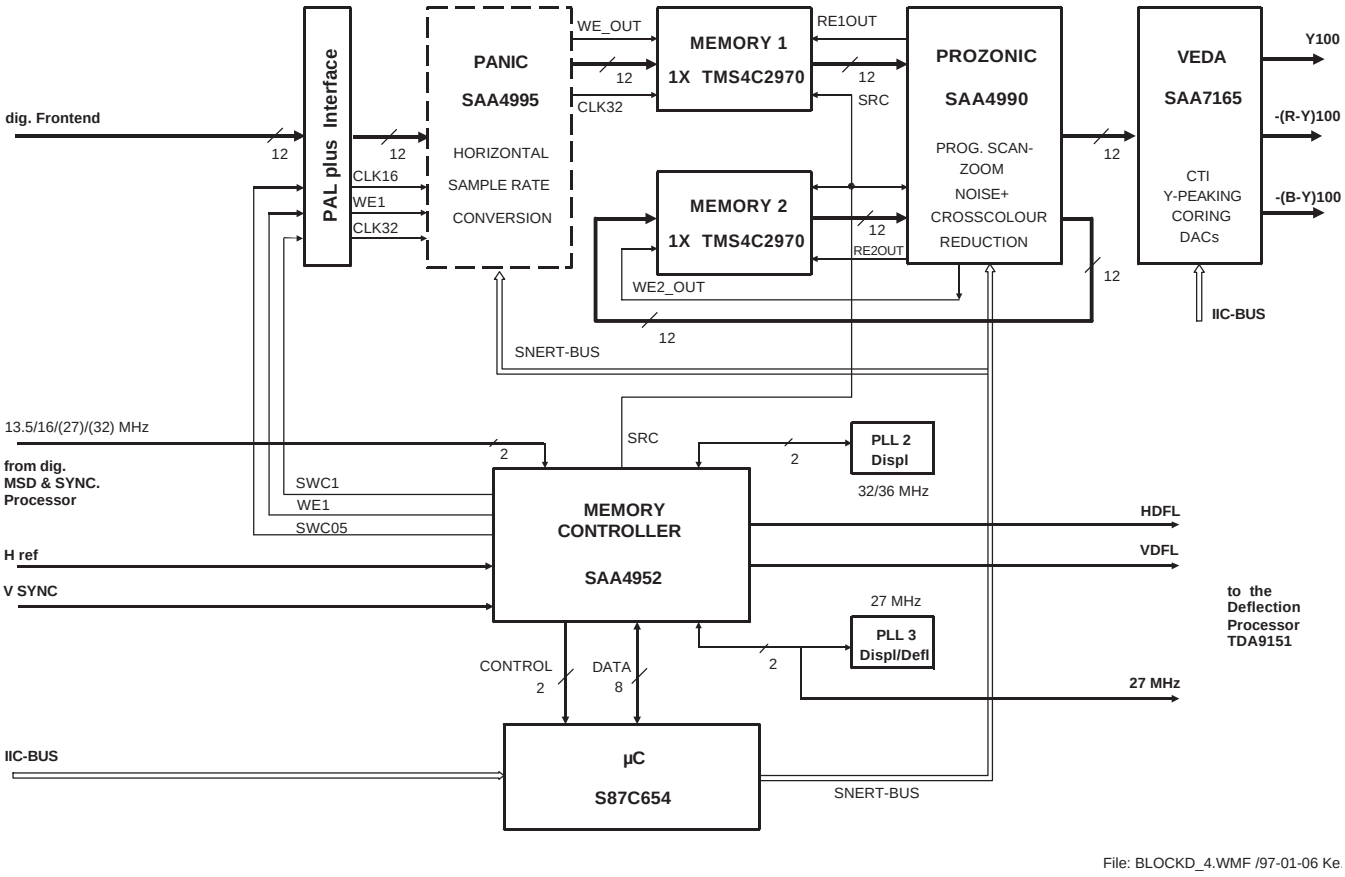


Fig.4 Block diagram of the IPQ Module for direct signal supply from a digital Multi-Standard Decoder and Sync. Processor IC.

The block diagram above shows the IPQ module implemented in a system with a digital colour decoder. In this case a clock signal provided by the digital decoder is used as acquisition clock. The memory controller is supplied with a horizontal reference pulse used to reset the H-counters in the SAA 4952. The digital data bus can directly be connected to the PANIC or to the first field memory if the PANIC is not implemented . If the deflection processor TDA 9151 is used, the display PLL 2 is necessary. This additional PLL can be left out when the TDA 9152 is used instead of TDA 9151.
If the user does not want to use the benefits of a double clock system, it is also possible to supply the whole system with a clock of 27 or 32 MHz. In this case no external PLL circuits are required. The controlling of the SAA 4952 can be adapted to this configuration by a special software.

3. Signal path of the SAA 4990 PROZONIC

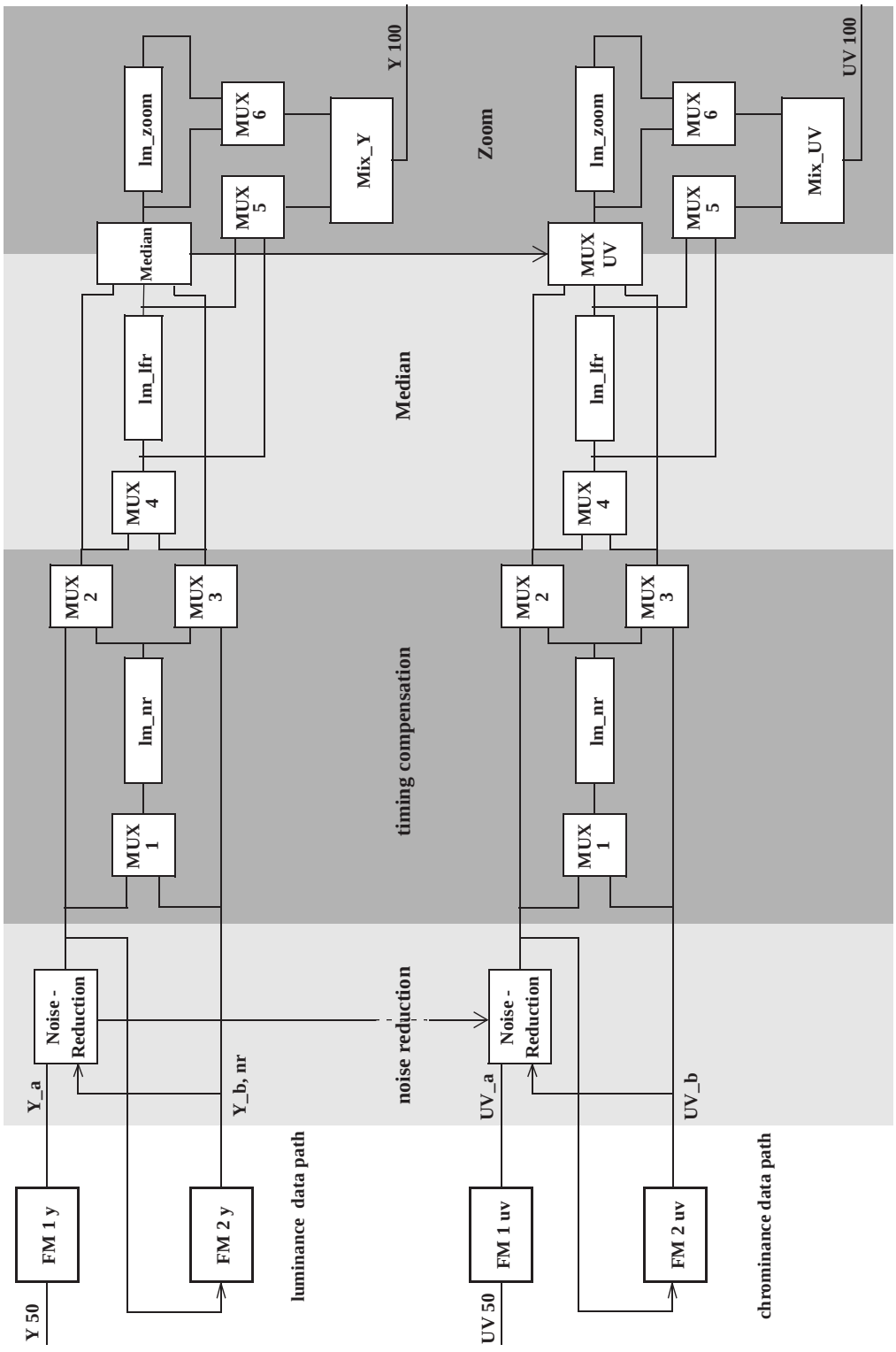


Fig.5 Main signal paths of PROZONIC

The block diagram of figure 5 shows the main signal paths of PROZONIC. The first processing block, directly connected to the field memories, is the noise reduction. The reading of the memories has to be adapted to the demands of the noise reduction timing in order to ensure that the same pairs of adjacent lines of a frame can be processed every 100 Hz field. If necessary also the signal data from one of the memories can be delayed by one line (lm_nr), thus the adjacent lines out of two fields are supplied into the following median filter block. The line memory lm_lfr is needed as a line delay for the median filter, which filters two adjacent lines from one field and the line in between from the other field. The settings of the multiplexers are defined by the software control. These settings are dependent on the selected field control mode and the field to be processed. The last processing part is the zoom block. The mixer can mix information from two lines with weighting factors. The input lines can contain median filtered and original unfiltered information.

4. General software description

The specification describes the functional requirements of an IPQ S87C654/P83C654FBA slave microcontroller software [1]. The slave IPQ µC is used as an interpreter between a main (master) µC and the ICs ECO4 (SAA4952), PANIC (SAA 4995) and PROZONIC (SAA 4990).

The IPQ µC reads up to 22 register bytes via the I²C bus from the master µC and sends itself 3 read bytes (1 status byte and 2 movie phase detection bytes) whenever addressed with R/W = 1. The I²C register bytes are written into the µCs RAM.

After the evaluation of data and following VDFL the IPQ µC sends data to ECO4 on port P0 (parallel), to PANIC and PROZONIC via the SNERT interface running in mode 0.

The VEDA is controlled directly via I²C-bus.

4.1 Main functional flow chart

After power-on reset the µ-controller performs an initialization. Romtable values are copied into RAM, control mode flags/variables are set/cleared. The VDFL interrupt has the highest priority. After initialization the main program waits for an occurring interrupt. During the initialization phase (after power on reset) the first VDFL interrupt is initiated by software.

After a VDFL interrupt has occurred on the µC port pin INT0N, the field number is read by the IPQ µC from the SAA 4952. Then the data transmission to PANIC, ECO4 and PROZONIC is performed. If the internal MPIP is used in an IPQ concept without PANIC (SAA 4995) the µ-controller is interrupted by the vertical acquisition synchronization pulse VACQ at INT1N instead of VDFL. This interrupt is also used in the generator mode. The field length of the display is constant and independent from the source if this option is active.

I²C input registers received during slave receiver operation are read and evaluated according to different priorities. The INIT bit in REG2 has the highest priority. If this bit is set, an initialization of ECO4/PANIC/PROZONIC with default values out of the µCs ROM table is done immediately. After VDFL interrupt handling, I²C interrupts can be serviced.

The I²C bus interrupt routine handles the reception of the register bytes from the master µC as well as the transmission of the status byte plus movie detection bytes.

The following flow chart shows the priority structure of the field control modes. The generator mode has the highest priority, followed by Multi PIP, Progressive Scan Mode and Sat Mode. The next levels in priority are the Auto-Movie Processing, the LFR Mode and on the lowest level the field repetition mode. The field control modes are described in detail in chapter 6.

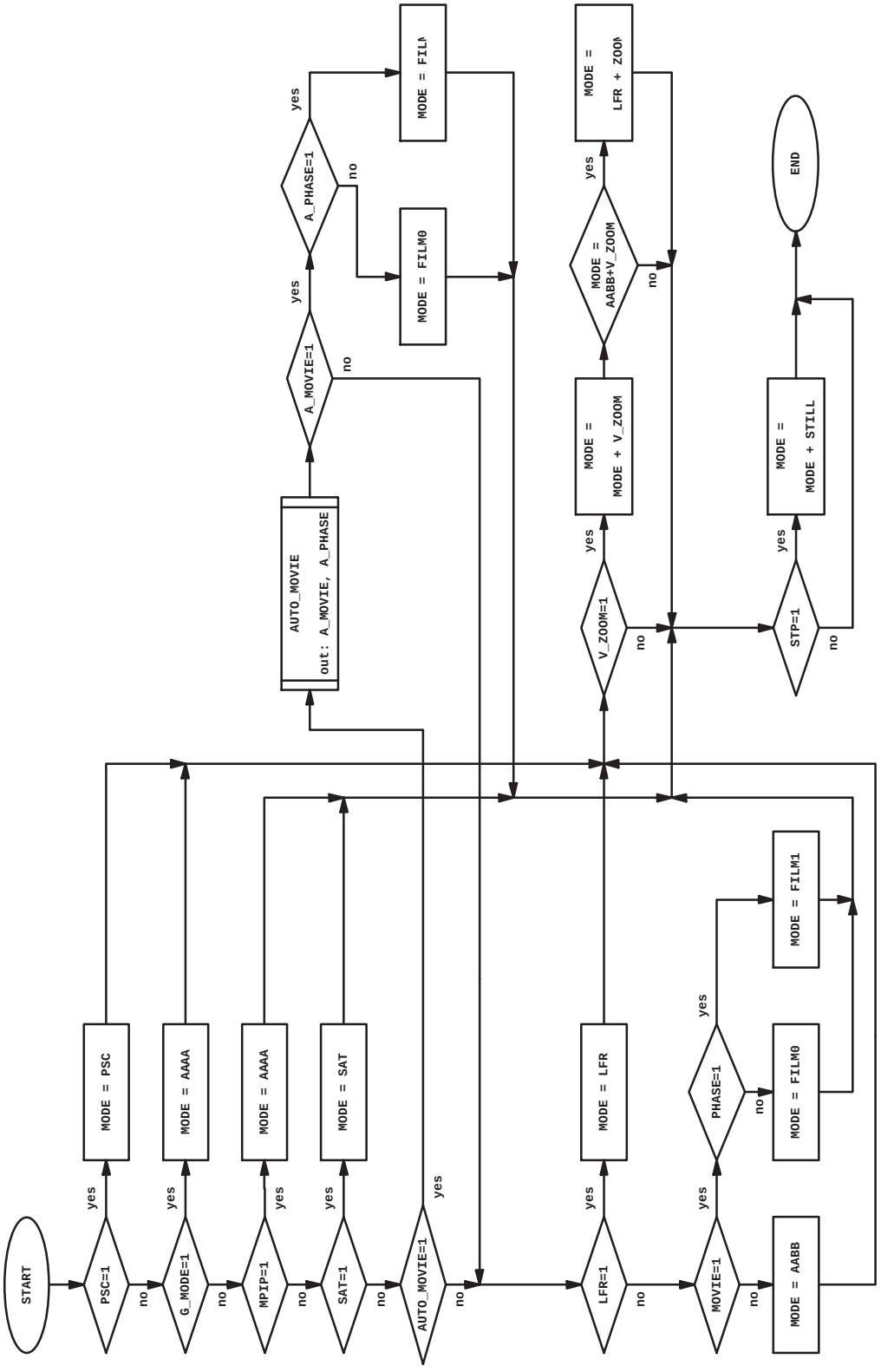


Fig.6 Software flow chart showing the priority structure of the field control modes

5. I²C-bus interface

5.1 Definition of the interface

The interface of the IPQ µC is realized with a hardware I²C bus [2].

The slave address of the IPQ µC is 68h:

Slave address = 0 1 1 0 1 0 0 R/W

The IPQ µC can either act as a slave receiver or a slave transmitter. In the slave receiver mode the IPQ µC reads I²C register data bytes from the main controller which then acts as a master transmitter. In the slave transmitter mode the IPQ µC sends status information plus 2 movie detection bytes to the main µC which works as a master receiver reading the byte information.

5.2 Sending data to the IPQ µC

5.2.1 I²C transmission protocol

The transmission protocol has the following format:

Start	Slave address	Ack	REG1	Ack	....	Ack	REG22	Ack	Stop

After having addressed the IPQ µC with its slave address the master µC transmits up to 22 register bytes over the I²C bus.

The control of some functions is different dependent on the fact whether the SAA 4995 (PANIC) is part of the system or not. Therefore this case the relevant I²C registers are listed twice, with PANIC and without PANIC.

I²C register data format

TABLE 1 I²C-Register REG1 (Conversion mode selection)

Bit	Name	Function
0	PSC	0: Progressive scan mode off 1: Progressive scan mode on
1	GENERATOR_MODE	0: normal mode 1: Generator mode on (312,5 lines / field continually)
2	SAT	0: Satellite mode off 1: Satellite mode on (A*A*B*B*)
3	reserved	

TABLE 1 I²C-Register REG1 (Conversion mode selection)

Bit	Name	Function
4	AUTO_MOVIE	0: movie detection disabled 1: automatic movie source detection activated. In case a movie mode is detected, a movie will be processed (MOVIE, MOVIE_PHASE are readable via STATUS register).
5	LFR	0: Line Flicker Reduction mode off 1: Line Flicker Reduction mode on
6	MOVIE	0: forced MOVIE mode off 1: forced MOVIE mode on
7	MOVIE_PHASE	forced phase flag to be set in combination with MOVIE: 0: normal (ABAB) 1: 180° phase shift (BCBC)

TABLE 2 I²C-Register REG2 (Field control)

Bit	Name	Function		
0	PP0	picture position bit 0		
1	PP1	picture position bit 1		
		PP1	PP0	picture position
		0	0	centre
		0	1	max. left
		1	0	max right
2	AFF	acquisition field frequency (50/60 Hz): 0: 50 Hz 1: 60 Hz		
3	STP	still picture mode: 0: off 1: on (one field out of AABB, full frame median filtered out of LFR)		
4	reserved			
5	reserved			
6	reserved			
7	INIT	initialize ECO4, PROZONIC, PANIC: 0 = off, 1 = on		

TABLE 3 I²C-Register REG3 (Vertical Zoom, Field control) (without PANIC)

Bit	Name	Function			
0	VZOOM_0	Vertical zoom bit 0			
1	VZOOM_1	Vertical zoom bit 1			
2	VZOOM_2	Vertical zoom bit 2			
		V2	V1	V0	Conversion factor
		0	0	0	no Zoom
		0	0	1	1,1
		0	1	0	1,25
		0	1	1	1,33
		1	0	0	1,5
		1	0	1	reserved
		1	1	0	reserved
		1	1	1	reserved
3	reserved				
4	FSA0	frequency select acquisition bit 0			
5	FSA1	frequency select acquisition bit 1			
		FSA1		FSA0	acquisition frequency
		0		0	12 MHz
		0		1	13.5 MHz
		1		0	16 MHz
		1		1	18 MHz
6	FSD0	frequency select display bit 0			
7	FSD1	frequency select display bit 1			
		FSD1		FSD0	display frequency
		0		X	27 Mhz
		1		0	32 MHz
		1		1	36 MHz

TABLE 4 I²C-Register REG3 (Vertical Zoom) (with PANIC)

Bit	Name	Function			
0	VZOOM_0	Vertical zoom bit 0			
1	VZOOM_1	Vertical zoom bit 1			
2	VZOOM_2	Vertical zoom bit 2			
		V2	V1	V0	Conversion factor
		0	0	0	no Zoom
		0	0	1	1,1
		0	1	0	1,25
		0	1	1	1,33
		1	0	0	1,5
		1	0	1	reserved
		1	1	0	reserved
		1	1	1	reserved
3	reserved				
4	reserved				
5	reserved				
6	reserved				
7	reserved				

TABLE 5 I²C-Register REG4 (Internal MPIP control) (without PANIC)

Bit	Name	Function
0	POS0	PIP position bit 0
1	POS1	PIP position bit 1
2	POS2	PIP position bit 2
3	POS3	PIP position bit 3
4	NPIP_4x4	0: no 4x4 PIPs, take NPIP 1: 4x4 PIPs

TABLE 5 I²C-Register REG4 (Internal MPIP control) (without PANIC)

Bit	Name	Function
5	NPIP	number of PIPs 0: 3x3 PIPs 1: 4x3 PIPs
6	MPIP	0: Multi-PIP off 1: Multi-PIP on
7	SPIP	NTSC PIP: 0: 50 Hz PIP 1: 60 Hz PIP

TABLE 6 I²C-Register REG4 (External MPIP control) (with PANIC)

Bit	Name	Function
0	POS0	PIP position bit 0
1	POS1	PIP position bit 1
2	POS2	PIP position bit 2
3	POS3	PIP position bit 3
4	NPIP_4x4	0: no 4x4 PIPs, take NPIP 1: 4x4 PIPs
5	NPIP	number of PIPs 0: 3x3 PIPs 1: 4x3 PIPs
6	MPIP	0: Multi-PIP off 1: Multi-PIP on
7	SPIP	NTSC PIP: 0: 50 Hz PIP 1: 60 Hz PIP

TABLE 7 I²C-Register REG5 (Noise reduction, split screen, screen fade, ect.)

Bit	Name	Function		
0	NR0	noise reduction bit 0		
1	NR1	noise reduction bit 1		
		NR0	NR1	noise reduction
		0	0	off
		0	1	low
		1	0	middle
		1	1	high
2	SPS0	split screen bit 0		
3	SPS1	split screen bit 1		
		SPS1	SPS0	split screen
		0	X	off
		1	0	horizontal
		1	1	vertical
4	SCF0	screen fade bit 0 (not yet implemented)		
5	SCF1	screen fade bit 1 (not yet implemented)		
		SCF1	SCF1	screen fade
		0	X	off
		1	0	fade in
		1	1	fade out
6	ENA_LFR_PHASE	0: fixed mode 1: adaptive control of LFR phase for movie sources		
7		reserved		

TABLE 8 I²C-Register REG6 (HWE1 delay)

Bit	Name	Function
0	HWE1F0	HWE1 fine delay offset to default, bit0
1	HWE1F1	HWE1 fine delay offset to default, bit1
2	HWE1F2	HWE1 fine delay offset to default, bit2
3	HWE1F3	HWE1 fine delay offset to default, bit3
4	HWE1F4	HWE1 fine delay offset to default, bit4
5	HWE1F5	HWE1 fine delay offset to default, bit5
6	HWE1F6	HWE1 fine delay offset to default, bit6
7	HWE1F7	HWE1 fine delay offset to default, bit7

TABLE 9 I²C-Register REG7 (Vertical shift)

Bit	Name	Function
0	VWE1D0	VWE1 delay bit 0
1	VWE1D1	VWE1 delay bit 1
2	VWE1D2	VWE1 delay bit 2
3	VWE1D3	VWE1 delay bit 3
4	VWE1D4	VWE1 delay bit 4
5	VWE1D5	VWE1 delay bit 5
6	VWE1D6	VWE1 delay bit 6
7	VWE1X	0: off, normal mode 1: on, vertical write window upwards shiftable by VWE1D0...D6

TABLE 10 I²C-Register REG8

Bit	Name	Function
0	SET_HOR_DEL	0: normal mode: HOR_DELAYS = 0 1: HOR_DELAYS value taken from REG12 direct PROZONIC access
1	SET_HDDEL	0: normal mode 1: take HDDEL setting from REG 13
2	SET_HD	0: normal mode 1: set HDSTA/STO ECO4 values direct via IIC REGs 14, 15
3	SET_VD	0: normal mode 1: set VDSTA/STO ECO4 values direct via IIC REGs 16, 17
4	SET_MSB	0: normal mode 1: take MSB setting from REG 18
5	reserved	
6	reserved	
7	reserved	

TABLE 11 I²C-Register REG9 (Port bit control)

Bit	Name	Function
0	reserved	
1	P11	0: clear port bit P1.1 1: set port bit P1.1
2	reserved	
3	P13	0: clear port bit P1.3 1: set port bit P1.3
4	P15	0: clear port bit P1.5 1: set port bit P1.5
5	P34	0: clear port bit P3.4 1: set port bit P3.4
6	P35	0: clear port bit P3.5 1: set port bit P3.5
7	P14	0: clear port bit P1.4 1: set port bit P1.4

TABLE 12 I²C-Register REG10: (Blank fields) (without PANIC)

Bit	Name	Function
0	BLANK_F0	Blank field 0
1	BLANK_F1	Blank field 1
2	BLANK_F2	Blank field 2
3	BLANK_F3	Blank field 3
4	reserved	
5	reserved	
6	reserved	
7	reserved	

TABLE 13 I²C-Register REG10: (Blank fields, PANIC control) (with PANIC)

Bit	Name	Function
0	BLANK_F0	Blank field 0
1	BLANK_F1	Blank field 1
2	BLANK_F2	Blank field 2
3	BLANK_F3	Blank field 3
4	PANIC_0	PANIC control bit 0
5	PANIC_1	PANIC control bit 1
6	PANIC_2	PANIC control bit 2
7	PANIC_3	PANIC control bit 3

TABLE 13 I²C-Register REG10: (Blank fields, PANIC control) (with PANIC)

Bit	Name	Function				
		P3	P2	P1	P0	mode
		0	0	0	0	normal mode
		0	0	0	1	hor. zoom factor 1,1
		0	0	1	0	hor. zoom factor 1,25
		0	0	1	1	hor. zoom factor 1,33
		0	1	0	0	hor. zoom factor 1,5
		0	1	0	1	hor. zoom factor 2
		0	1	1	0	reserved
		0	1	1	1	reserved
		1	0	0	0	hor. lin. compress factor 1,33
		1	0	0	1	PANORAMA mode, high non-linearity
		1	0	1	0	PANORAMA mode, moderate non-linearity
		1	0	1	1	reserved
		1	1	0	0	reserved
		1	1	0	1	reserved
		1	1	1	0	reserved
		1	1	1	1	reserved

TABLE 14 I²C-Register REG11 (Port bit and 27MHz PLL control)

Bit	Name	Function
0	P20	0: clear port bit P2.0 1: set port bit P2.0
1	P21	0: clear port bit P2.1 1: set port bit P2.1
2	P22 (TGSC)	0: clear port bit P2.2 1: set port bit P2.2
3	P23 (FILL)	0: clear port bit P2.3 1: set port bit P2.3

TABLE 14 I²C-Register REG11 (Port bit and 27MHz PLL control)

Bit	Name	Function
4	P24	0: clear port bit P2.4 1: set port bit P2.4
5	reserved	
6	reserved	
7	PLLMID (P27)	0: 27 MHz PLL locked 1: 27 MHz PLL free running

TABLE 15 I²C-Register REG12 (Horizontal delay)

Bit	Name	Function
0....7	HOR_DELAYS	direct PROZONIC register access

TABLE 16 I²C-Register REG13 (Horizotal fine delay)

Bit	Name	Function
0....7	HDDEL	direct ECO4 register access, fine delay of the hor. display signals

TABLE 17 I²C-Register REG14 (Start value of HD signal)

Bit	Name	Function
0....7	HDSTA	direct ECO4 register access, start value of the HD signal

TABLE 18 I²C-Register REG15 (Stop value of the HD signal)

Bit	Name	Function
0....7	HDSTO	direct ECO4 register access, stop value of the HD signal

TABLE 19 I²C-Register REG16 (Start value of the VD signal)

Bit	Name	Function
0...7	VDSTA	direct ECO4 register access, start value of VD signal, vertical blanking for DAC via ECO4 signal HVCD

TABLE 20 I²C-Register REG17 (Stop value of the VD signal)

Bit	Name	Function
0...7	VDSTO	direct ECO4 control register access, stop value of VD signal

TABLE 21 I²C-Register REG18 (MSD control)

Bit	Name	Function
0	MSB_HDSTA	MSB of SAA 4952 HD start value
1	MSB_HDSTO	MSB of SAA 4952 HD stop value
2	MSB_VDSTA	MSB of SAA 4952 VD start value
3	MSB_VDSTO	MSB of SAA 4952 VD stop value
4....7	reserved	

TABLE 22 I²C-Register REG19 (LIMERIC control, Taste)

Bit	Name	Function
0....7	TASTE	direct LIMERIC register access, SNERT address F3hex

TABLE 23 I²C-Register REG20 (LIMERIC control, Status)

Bit	Name	Function
0....7	STATUS	direct LIMERIC register access, SNERT address F4hex

TABLE 24 I²C-Register REG21 (LIMERIC control, Wanted Value)

Bit	Name	Function
0....7	WVAL	direct LIMERIC register access, SNERT address F5hex

TABLE 25 I²C-Register REG22 (LIMERIC control, Noise Estimator)

Bit	Name	Function
0....7	NOISE EST.	direct LIMERIC register access, SNERT address FAhex

5.2.2 Acknowledgement of bytes

The IPQ µC acknowledges always the 22 register bytes (maximum number) independent from their contents. If the master µC transmits more than 22 register bytes, the slave µC will not acknowledge the following bytes.

5.3 Receiving status information from the IPQ µC

The IPQ µC is able to transmit one status byte and the 2 motion sum registers to the main µC. The IPQ µC then works as a slave transmitter.

5.3.1 I²C transmission protocol

The I²C bus transmission protocol for transmitting the status byte has the following format:

Start	Slave address 69H	Ack	Status byte	Ack	motion sum A	Ack	motion sum B	NAck	Stop

5.3.2 Contents of status byte

The status byte contains the following information:

TABLE 26 Readregister 1, Statusregister

Bit	Name	Function
0	NON_IL	0: source with interlaced picture 1: non-interlaced source detected via software
1	SF_DONE	0: SCREEN FADE is active 1: SCREEN FADE is done
2	LFR_PHASE	0: LFR_PHASE=0 1: LFR_PHASE=1
3	MOVIE_FLAG	0: no movie source detected 1: movie source detected
4	MOVIE_PHASE_FLAG	the MOVIE_PHASE_FLAG information is only relevant if MOVIE is set; 0: normal movie phase relation (ABAB) 1: shifted movie processing (BCBC)
5	PORT24	bit setting read from port bit P2.4 0: P2.4=0 1: P2.4=1
6	READY	0: not ready to accept IIC commands 1: ready to accept IIC commands
7	WATCH	Watchdog bit; will be toggled when status byte is read by master µC, initialized with 0

TABLE 27 Readregister 2, (PROZONIC MPD MSByte A)

Bit	Name	Function
0...7	MOTION_SUM_A	MSByte of PROZONIC read register for SAD of luminance values per field, result for field A

TABLE 28 Readregister 3, (PROZONIC MPD MSByte B)

Bit	Name	Function
0...7	MOTION_SUM_B	MSByte of PROZONIC read register for SAD of luminance values per field, result for field B

The ready bit in the first byte will be cleared after the IPQ µC has received I²C register bytes. It will be set again after the evaluation of all bytes is completed and an external interrupt (VDFL from ECO4) initiating data transfer from IPQ µC to ECO4, PANIC, PROZONIC is not currently serviced.

5.4 Timing aspects

The maximum allowed response time between accepting register bytes and the execution of the commands handled by the IPQ µC is 90 ms. This time is only relevant when field memory control modes are changed. Field memory control modes are: Movie, Sat, LFR, Still, Multi-PIP mode. When a field memory control mode has been activated, the IPQ µC waits max. 40 ms until a new frame starts in LFR mode (4 x 100Hz field repetition time). Then it takes another 40 ms until one new frame has been completely transmitted in order to run the new mode.

The maximum allowed total clock stretch time of the IPQ µC within one I²C message is 5 ms.

The minimum wait time between sending two I²C bus register data packages varies from 12 ms (no field memory control modes have changed) to 90 ms (field memory control modes have changed).

If the user wants to make sure that a complete I²C bus register data package is transmitted without being interrupted by VDFL IRQ µC routine and the slave µC is free for I²C after the master µC transmits I²C data, the I²C data package should be transmitted between 3 and 5 ms after VDFL occurred. The slave µC sets bit 6 of the status byte when it is ready to accept I²C commands.

Multi-PIP:

The time between two I²C bus commands activating 2 different PIP picture positions should not be smaller than 120 ms.

Screen fade:

As long as this mode is active (86 fields = 860 ms in normal mode), all other mode changes are ignored.

6. Functional description

The functional description includes the description of all features of the IPQ module which can be controlled over the I²C-bus interface.

The evaluation of I²C bus register data is done with respect to a certain priority structure. The priotrity structure of the field memory control modes are shown in Fig. 6. In the following sections certain restrictions on bit settings in the I²C register bytes which limit the possibilities of combining field memory control modes (Movie, Sat, LFR, Still, Multi-PIP mode, Progressive Scan) and/or secondary control commands are listed (see chapter 5.2).

6.1 Field memory control modes

6.1.1 LFR mode

Software Control: IIC-Register 1, Bit 5 (LFR)=1

The Line Flicker Reduction Mode is the default control mode. It is activated if the control bit LFR is set. In this display mode the sequence of the four 100 Hz fields per input frame is built as follows:

The first field is the original field A. The second field is a median filtered field A*. The median filter uses two lines from field A and the line in between from field B as input information. The third output field B* is again median filtered. The inputs are derived from two lines taken from field B and the line in between from field A. The last field is the original field B.

Control mode: AA*B*B (ABAB display raster)

Restrictions: The LFR mode cannot be combined with:

MPIP (Multi-PIP)

GENERATOR Mode

Disabled modes: AABB mode, forced MOVIE mode

Combination exclusions secondary control modes: none

6.1.2 AABB mode

Software Control: IIC-Register 1 = 0H

This mode is the field memory control mode which is active if no field mode control bits have been set (lowest priority). It is the most simple 100 Hz conversion mode. Only the first field memory is necessary for the field doubling. For low cost concepts it is possible to leave out the PROZONIC. The software control supports both hardware configurations with or without PROZONIC (VRE1 control).

Control mode: AABB (AABB display raster)

Restrictions: The AABB mode cannot be combined with:

MPIP (Multi-PIP)

GENERATOR Mode

Disabled modes: none

Combination exclusions secondary control modes: none

6.1.3 Movie mode

Software Control: IIC-Register 1, Bit 6 (MOVIE)

The MOVIE mode is foreseen for a movie source where the time resolution is only 25/30 Hz. In this case the median filter of PROZONIC can be switched off and a simple ABAB display is shown (frame repetition). The sequence of the video fields (odd/even) is not defined in relation to the movie pictures. So the IPQ µC has to find out whether a movie transmission takes place and in which phase relation it is transmitted. A forced activation of the MOVIE mode in case of a video source transmission would cause severe movement effects.

Control mode: ABAB, display raster ABAB

Activation/restrictions: It is activated if the MOVIE bit is set and the bit AUTO_MOVIE is cleared (forced MOVIE mode). In case AUTO_MOVIE is set the mode is only active if the software routine has detected a movie source (automatic movie detection routine). The result of the movie detection is copied to the status byte.

MOVIE mode does not run in the Multi-PIP mode.

Disabled modes: AABB mode

Combination exclusions secondary control modes: none

6.1.4 Phase adaption for the movie processing

Software Control: IIC-Register 1, Bit 7 (MOVIE_ PHASE)

The Phase bit can be set in combination with the bit MOVIE. It determines the phase relation for the frame repetition in relation to the incoming fields. The converter performs an ABAB conversion if MOVIE_PHASE is cleared and a BCBC conversion if MOVIE_PHASE is set.
The forced movie mode can be used in case of a PALplus transmission where the information whether a movie is transmitted or not can be derived from a special information line.

Control mode: ABAB for MOVIE_PHASE = 0, BCBC for MOVIE_PHASE = 1 raster (field phase is shifted).

Activation/restrictions: It is activated if the MOVIE_PHASE bit is set. If the bit is cleared the display raster is the normal ABAB.

Combination exclusions secondary control modes: none

6.1.5 Automatic movie mode detection

Software Control: IIC-Register 1, Bit 4 (AUTO_MOVIE)

In the automatic movie mode (AUTO_MOVIE=1) the phase information is generated by the software internally and the control bit MOVIE_PHASE has no influence. Via the status register the phase information can be read. It is coded in the bit PHASE_Flag.

The bit AUTO_MOVIE activates the software routine to detect whether a video or movie source has to be 100 Hz converted. Furthermore the phase relation between video (odd/even) and movie picture has to be calculated.

Activation/restrictions: It is activated if the AUTO_MOVIE bit is set.

The movie detection is based on measurements of absolute luminance differences between successive input fields, pixel by pixel. These differences are summed over the whole active field and deliver a result every field which can be read by the µ-controller. In case of a film source with sufficient movement, the measurement results will alter from field to field between high and low values. The microprocessor filters this data (low pass loops) and generates the movie and phase information.

Combination exclusions secondary control modes: none

6.1.6 Automatic LFR phase adaptation

Software Control: IIC-Register 5, Bit 6 (ENA_LFR_PHASE)

If a movie source is 100 Hz converted in the LFR mode (median based field interpolation) the motion effects in e.g. vertically scrolling text information can be reduced, if the LFR sequence AA*B*B is controlled with the correct phase relation to the original movie picture.

Activation/restrictions: If the bit ENA_LFR_PHASE is set a phase adaptation of the LFR sequence for movie sources is performed. If the bit is cleared, the LFR sequence is fixed according the field recognition of the memory controller.

The movie detection in this mode works similar to the automatic movie detection. The only difference is that the processing times implemented in the software are longer, because the movie detection does not have to decide very quickly.

There is no need to switch between MOVIE and LFR mode. The LFR mode is activated always, only the phase relation of the LFR sequence towards the video fields (even / odd) is changed if necessary.

Combination exclusions secondary control modes: none

6.1.7 Generator mode

Software Control: IIC-Register 1, Bit 1 (GENERATOR_MODE)

The bit GENERATOR_MODE activates a stable 100 Hz display with a fixed field length of 312.5 lines. The display field length is not adapted to the video source. If additionally the 27 MHz PLL is unlocked via the control bit PLLMID the display is also in a horizontally free running mode. The conversion mode is reduced to a four times single field repetition (AAAA) in this unsychronized mode. This special mode can be used to get a stable OSD picture without a source or with a very noisy source. It does also improve the picture stability for a tuner channel search.

6.1.8 Satellite mode

Software Control: IIC-Register 1, Bit 2 (SAT)

In the satellite mode all the four 100 Hz display fields are derived from the output of the median filter. The median filter filters out details occurring in only one line. This fact can be used to suppress typical FM noise dropouts which normally occur uncorrelated in the field. A bad satellite signal reception can be improved quite effectively in this mode without deteriorating the picture quality.

Control mode: A*A*B*B* (display raster AABB)

Activation/restrictions: Satellite mode is activated if the SAT bit is set. LFR, CINE mode or AABB display raster doesn’t run in Satellite mode.

6.1.9 Progressive Scan Mode

Software Control: IIC-Register 1, Bit 0 (PSC)

Control mode: 50/60 Hz, 1250/1050 lines (display raster: non-interlaced)

If the bit PSC is set a progressive scan mode is activated. The de-interlacing function (line interpolation) is performed with the help of the PROZONIC median filter. This mode could be preferably used for NTSC sources. The number of lines per field (525 lines / 60 Hz) is doubled and additionally the line flicker is removed. For NTSC

sources a reduction of the visibility of the line structure is more important than the reduction of large area flicker (60/120 Hz) because a 60 Hz display shows much less large area flicker than a 50 Hz display.

Activation/restrictions: It is activated if the PSC bit is set.

Disabled modes:
- Movie mode
- LFR mode
- AABB mode

Combination exclusions secondary control modes: none

6.1.10 Multi-PIP

Software Control: IIC-Register 4, Bit 6 (MPIP)

The Multi-PIP feature uses the field memories of the 100 Hz converter to generate or to support a Multi-PIP display. This function can be used for channel overview or photo-finish. Photo-finish shows a sequence of frozen pictures of one source stored with constant time steps. If the PANIC is implemented in the 100 Hz module an external PIP module is necessary. The PIP display is assumed to be positioned at the bottom right of the screen. The PIP information is written to the desired MPIP position in the memory.

If no PANIC is implemented there are two possibilities to implement the MPIP function. The first possibility is described above. For low cost concepts the internal MPIP function of the memory controller SAA 4952 can be used alternatively. In this case no external PIP-Module is required. The PIP pictures however are generated without appropriate filtering and show aliasing effects if the input pictures have a lot of details.

Function:

Multi picture-in-picture active for MPIP = 1, 3x3 MPIP for NPIP=0; 4x3 for NPIP=1 (external PIP) or 4x4 for NPIP=1 (internal PIP processing)

The positions are chosen via the bits POS0 to POS3

Combination exclusions secondary control modes: not combinable

6.1.11 Still picture

Software Control: IIC-Register 2, Bit 3 (STP)

It is possible to activate a still picture function in every control mode of the scan converter. The processing of this option is adapted to the conversion mode being activated before.

Control mode:
a) AA*AA* (full frame median filtered)
b) AAAA (single field control)
c) ABAB
d) PSC (frame based still picture)

The display raster in still picture is always ABAB.

Activation/restrictions: It is activated if the STP bit is set.

Disabled modes: none

Combination exclusions secondary control modes: none

Detail information:

If Still picture is performed while Noise reduction is active, a noise reduced frozen picture will be displayed.

Still picture mode at the different display modes:

Normal mode (AABB) Still Picture mode => AAAA

LFR mode (AA*B*B) Still Picture mode => AA*AA*

MOVIE mode(ABAB) Still Picture mode => ABAB

SAT mode (A*A*B*B*) Still Picture mode => A*A*A*A*

6.1.12 Vertical Zoom Function

Software Control: IIC-Register 3, Bits 0 to 2 (VZOOM_0 to VZOOM_2)

Activation: It is activated if the VZOOM bit is set. The bits VZOOM_0 to VZOOM_2 determine the zoom factor according to the I^2C register table of REG3.

Four different vertical zoom modes are implemented. These zoom factors are 1.1, 1.27, 1.33, 1.5 and 2.0.

The vertical sample rate conversion of PROZONIC can cope with the various letterbox formats. The sample rate conversion is performed on adjacent lines of a frame, the frame information consists of original and median filtered lines. This feature is used to display sources with e.g. 16:9 or 14:9 aspect ratios on 4:3 displays without side panels.

6.2 Secondary control commands

6.2.1 General

Secondary control commands are:
(*: all combinable)

- Frequency selection/picture position
- Acquisition field frequency (*)
- Noise reduction
- Split screen
- Screen fade
- Peaking (*)
- CTI
- Port settings
- Initialization command
- HWE1 fine delay setup control (*)
- VWE1 delay setup control (*)

6.2.2 Frequency selection (only on modules without SAA 4995, PANIC)

Software Control: IIC-Register 3, Bit 4 to 7 (FSA0, FSA1 and FSD0, FSD1)

Function: Selection of the horizontal conversion mode (horizontal compression or zoom factor)

The following frequency combinations will be accepted by the IPQ µC:

acquisition frequency [MHz]	display frequency [MHz]	mode	compression/ zoom factor [%]
12	32	compress	33
13.5	27	normal	-
13.5	32	compress	19
13.5	36	compress	33
16	27	zoom	19
16	32	normal	-
16	36	compress	12.5
18	27	zoom	33
18	32	zoom	12.5

All compression modes can be displayed in centre picture position max. right or in max. left position. The picture position is selected by setting/clearing the PP bits PP0 and PP1.

Combination exclusions:

PANIC application: PANIC replaces all these zoom functions, details see section below.

6.2.3 PANIC control (only relevant if the SAA 4995 is implemented)

Software Control: IIC-Register 10, Bit 4 to 7 (PANIC_0 to PANIC_3)

Function: 4 different horizontal zoom factors, two different compression modes and a non linear PANORAMA mode are selectable by these four bits, see table below.

PANIC control modes:

TABLE 29

P3	**P2**	**P1**	**P0**	**mode**
0	0	0	0	normal mode
0	0	0	1	hor. zoom factor 1.1
0	0	1	0	hor. zoom factor 1.25
0	0	1	1	hor. zoom factor 1.33
0	1	0	0	hor. zoom factor 1.5

TABLE 29

P3	P2	P1	P0	mode
0	1	0	1	hor. zoom factor 2
0	1	1	0	reserved
0	1	1	1	reserved
1	0	0	0	hor. linear compress factor 1.33
1	0	0	1	Panorama mode (high non-linearity)
1	0	1	0	Panorama mode (moderate non-linearity)
1	0	1	1	reserved
1	1	0	0	reserved
1	1	0	1	reserved
1	1	1	0	reserved
1	1	1	1	reserved

6.2.4 Acquisition field frequency

Software Control: IIC-Register 2, Bit 2 (AFF)

Function:

The acquisition field frequency can be switched to 60 Hz by setting the AFF bit in REG1. The software stops the vertical writing window adapted to the NTSC field length. The software detects if the number of lines per field of incoming source is according to the chosen standard (lines per field). If the field length differs by more than 3 lines the converter activates a single field 100 Hz conversion (AAAA). This improves the quality of VCRs in trick modes (fast forward, fast backward) compared to 50 Hz receivers. To have a correct switching from the normal mode to the single field mode the AFF bit has to controlled according to the source.

Dependencies/exclusions: None

6.2.5 Initialization command

Software Control: IIC-Register 2, Bit 7 (INIT)

Function:

If the INIT bit is set, the ECO4 and PROZONIC default values in the µC ROM are transmitted to these ICs. A live video picture will be displayed with compression/zoom off, line flicker reduction switched on.

6.2.6 Noise reduction

Software Control: IIC-Register 5, Bit 0 and 1 (NR0, NR1)

Function:

3 different adaptive noise reduction curves are selectable via the I^2C bus. These setting are also relevant for the amount of noise reduction when activating split screen.

Combination exclusion: None

Activation: It is activated if one of the bits NR0 or NR1 is set, see table.

Noise reduction setting:

Noise reduction	“Off”	NR1=0	NR0=0
Noise reduction	“Low”	NR1=0	NR0=1
Noise reduction	“Middle”	NR1=1	NR0=0
Noise reduction	“High”	NR1=1	NR0=1

The noise reduction is based on recursive filtering. The recursive filter loop is built up in the $2f_H$ domain. The second field memory serves as the required field delay and contains the noise reduced picture. The ratio between recirculated information and new data from the incoming source is adapted via a motion detector automatically. The motion detection bases on the investigation of luminance differences (absolute differences) calculated between the output of memory 1 (new data) and the old data from memory 2.

6.2.7 Split screen function

Software Control: IIC-Register 5, Bit 2,3 (SPS0, SPS1)

The split screen command declares a box in which the currently active adaptive noise reduction is enabled whereas the rest of the screen is displayed with noise reduction switched off. The box may split the screen display in two halves horizontally or vertically. Split screen will not be activated if noise reduction is switched off.

Combination exclusions: compress, screen fade (Split screen has lower priority than screen fade.)

6.2.8 Screen fade function

Software Control: IIC-Register 5, Bit 4, 5 (SCF0, SCF1), (Not yet implemented!)

The screen fade feature can be used to “fade out” a picture like closing curtains. This is done by the control SW by continuously changing the setting of the horizontal blanking for the DAC until a completely black picture is visible. The function is also available the other way round where the picture is “faded in” starting from a black display.

Screen fade has a higher priority than split screen.

Combination exclusions: see main functional flow chart

6.2.9 µC port control

Software Control: IIC-Register 9, Bit 1, 3 to 7 (P11, P13, P15, P34, P35 and P14), IIC-Register 11 Bit 0 to 4 and 7 (P20, P21, P22, P23, P24 and P27)

Function:

This function enables the µC master to set/clear IPQ port bits via the I²C bus. The port bit P2.4 is reflected to bit PORT, STATUS register:
The port pin P2.4 is read in order to check whether the bit is held low by an external device.

Combination exclusions: None

6.2.10 Prozonic control byte HOR_DELAYS

Software Control: IIC-Register 8, Bit 1 (SET_HOR_DEL)

Function: Direct PROZONIC register access via I²C-bus.
If the control bit SET_HOR_DEL is set the PROZONIC control byte HOR_DELAYS (SNERT address 1Eh) can be directly accessed via I²C-bus register REG12.
The bits 0 to 2 determine the horizontal delay (0 to 7 clock periods) of the luminance data in relation to the U/V input data from field memory 1.
The bits 3, 4 determine a pulse shift with clock accuracy (1 to 4 clocks) for the horizontal reference signal (HREF). This setting has to be programmed in a way that the internal reformatting of the 4:1:1 colour difference data does not fail.
The bits 5, 6 determine a pulse shift (1 to 4 clocks) for the write enable output signal (WE2_OUT). The signal WE2 has to ensure that the data being read from memory 1 are written correctly into the second field memory.

6.2.11 HDDEL control

Software Control: IIC-Register 8, Bit 1 (SET_HDDEL)

If the control bit 1 of IIC register 8 is set, a direct access to the SAA 4952 HDDEL register is enabled via the IIC register 13. The HDDEL register allows to delay the horizontal display signals to be delayed with clock accuracy. The signals concerned are HRE, HWE2, BLND and HD.

6.2.12 HD control

Software Control: IIC-Register 8, Bit 2 (SET_HD)

If the control bit 2 of IIC register 8 is set a direct access to the SAA 4952 HD start and stop registers is enabled via IIC registers 14, 15. A completely new definition of the signals can be achieved in combination with the control bytes HDSTA and HDSTO. MSB control can be executed by the bits MSB_HDSTA and MSB_HDSTO via the IIC register 18, details see section MSB control.

6.2.13 VD control

Software Control: IIC-Register 8, Bit 3 (SET_VD)]

If the control bit 3 of IIC register 8 is set a direct access to the SAA 4952 VD start and stop registers is enabled via IIC registers 16, 17. A completely new definition of the signals can be achieved in combination with the control bytes VDSTA, VDSTO. MSB control can be executed by the bits MSB_VDSTA and MSB_VDSTO via the IIC register 18, details see section MSB control.

6.2.14 MSB control

Software Control: IIC-Register 8, Bit 4 (SET_MSB)

If the control bit 4 of IIC register 8 is set a direct access to the SAA 4952 MSB register is enabled via the IIC register 18. The MSB register defines the MSBs of the 9 Bit start and stop values of the horizontal display signals HD, HRE and HWE2 and the vertical display signals VRE1, VRE2, VWE2 and VD.

6.2.15 HWE1 delay function

Software Control: IIC-Register 6, Bits 0 to 7 (HWE1F0 to HWE1F7)

Function:

By changing the bits HWE1F0..HWE1F7, the default value of the HWE1STA/STO can be modified.
The default value is defined with 42 Hex by the IPQ control software. This default value can be either decremented or incremented step by step within the range of 00 Hex to 84 Hex. A time correction of 1 acquisition clock cycle is achieved per control step.
For fine adjustment of the processing timing it can be useful to start from the default setting (HWE1F0.HWE1F7 = 42 Hex) and altering the value by I²C bus.

6.2.16 VWE1 delay function

Software Control: IIC-Register 7, Bits 0 to 7 (VWE1D0 to VWE1D6 and VWE1X)

If the bit VWE1X is set to 1, the start of vertical writing window can be delayed via the control bits VWE1D0...D6. In case VWE1X = 0, the normal mode (default vertical write window) is processed.

6.2.17 Field blanking function

Software Control: IIC-Register 10, Bits 0-3, (BLANK_F0 - BLANK_F3)

The Blank Field Mode allows the user to define which fields of the sequence of the 100 Hz display fields are displayed or blanked. If the AABB mode is active a blanking of every second field generates a display which is similar to a standard 50 Hz projection. The elimination of the large area flicker can be demonstrated by switching from this mode to a normal 100 Hz display.

6.2.18 NPIP_4x4

Software Control: IIC-Register 4, Bit 4 (NPIP_4x4)

Function: 4x4 PIP for external PIP modules

This bit enables the external 4x4 PIP display. This bit has a higher priority than the control bit NPIP in I²C register 4.

6.2.19 SPIP

Software Control: IIC-Register 4, Bit 7 (SPIP)

The field frequency of the PIP processing is defined by the bit SPIP. The timing of the PIP processing can be adapted to a 50Hz or 60Hz field frequency. If the bit SPIP is set to 1, NTSC PIP is selected and the timing is adapted to 60Hz field frequency.

6.2.20 P23 (FILL)

Software Control: IIC-Register 11, Bit 3 (P23 or FILL)

Function: Generation of a constant fill or background colour.

If the fill bit is set the ADC outputs are disabled. Via pull-up or pull-down resistors a constant luminance and colour difference value can be forced on the data bus. This constant data can be stored in the memories of the up-converter to obtain a background for the Multi-PIP display or to have a desired background for display on screen applications.

6.2.21 P27 (PLLMID)

Software Control: IIC-Register 11, Bit 7 (P27 or PLLMID)

Function: Decoupling of the 27 MHz PLL (free-running PLL)

Via the control bit PLLMID the deflection PLL can be set into a free-running mode. In this case the display is decoupled from the horizontal reference. In combination with the generator mode the display can be completely decoupled from the source. This mode is necessary for the internal Multi-PIP where the display has to be stable in case of switching the source.

6.2.22 Taste register (LIMERIC, SAA 4945)

Software Control: IIC-Register 19 (TASTE)

Function/restrictions:

Direct LIMERIC register access of address F3hex. For LIMERIC application only!

Details see data sheet of LIMERIC. The taste factor defines the amount of noise reduction processed by the LIMERIC. The taste control has a linear influence on processing.

6.2.23 Status register (LIMERIC)

Software Control: IIC-Register 20, (STATUS)

Function/restrictions:

Direct LIMERIC register access of address F4hex. For LIMERIC application only!

Details see data sheet of LIMERIC. Via this register for example a split screen feature can be activated.

6.2.24 WVAL, wanted value (LIMERIC)

Software Control: IIC-Register 21, (WVAL)

Function/restrictions:

Direct LIMERIC register access of address F5hex. For LIMERIC application only. The register setting sets up the noise estimator.

Details see data sheet of LIMERIC.

6.2.25 NOISE EST. setting register (LIMERIC)

Software Control: IIC-Register 22, (NE)

Function/restrictions:

Direct LIMERIC register access of address FAhex. For LIMERIC application only. Via the register prefilter settings for the noise estimator can be changed.

Details see data sheet of LIMERIC.

7. SNERT and Parallel interface

Via the SNERT and the Parallel interface all register data for PANIC, PROZONIC and ECO4 is transmitted [3].

7.1 SNERT interface

All register data to PANIC and PROZONIC is transmitted/received via the SNERT interface of the IPQ µC.

7.1.1 PANIC data transmission/receiption

The IPQ µC sends 9 registers to PANIC after every second VDFL synchronized to the incoming fields.

7.1.2 PROZONIC data transmission

The IPQ µC sends after each VDFL 17 registers to Prozonic.

The IPQ µC transmits only one of the two registers Vbox_start_l and Vboxstart_h according to the setting of bit 8. The same applies for the registers Vboxstop_l and Vbox_stop_h.

7.2 Parallel interface

Here all 25 ECO4 register data bytes are transmitted.

The read/write from/to the ECO4 is done according to the read/write operation to external memory specified in the data sheet of the IPQ µC.

The signals WRN and RDN of the IPQ µC are wired OR connected to WRD, ECO4. ALE is directly connected to ECO4.

8. Function control of VEDA (SAA 7165)

All VEDA functions like Peaking, Coring and CTI are directly controlled via I^2C-bus by the master µC.

The slave address is 1011 111X
X = R/$\overline{W}$ control bit
a) X = 0, order to write (device is slave receiver)
b) X = 1, order to read (device is slave transmitter)

8.1 Y,U,V input data format

The Y,U,V input data format is 4 : 1 : 1 and two´s complement data code with 8 bit chrominance signal resolution in the IPQ board. This data format has to be selected for VEDA.

U, V input signal data:

4 : 1 : 1 data format is processed, if the IFF bit in subaddress 02 is cleared.
Two´s complement data code is selected if the DRP bit is cleared.
8 bit chrominance resolution is processed if the R78 bit is set (subaddress 03).

Remark: VEDA is able to handle both, 4 : 1 : 1 and 4 : 2 : 2 Y,U,V data with 7 or 8 bit chrominance resolution.

Y input signal data:

A blanking level of 0 LSB has to be set for the Y output DAC. This is achieved if the bit BLV is set (subaddress 03).

Default bit addressing for VEDA, without Peaking and Coring but active CTI function:

TABLE 30

Subaddress	Data in Hex
01	00
02	03
03	06

8.1.1 Peaking

Function:

Transversal filtering is applied to the Y signal (data). Peaking increases the amplitude frequency response of the Y signal in certain frequency range. Furthermore it modifies the transient signal response due to linear phase filtering.

By means of peaking, the bandwidth reduction due to attenuations in the signal path can be compensated on the Y signal.

Y signal peaking is provided with 4 different degrees. The characteristic transversal filter can be modified too, see bit explanation below.

The degree of peaking is selectable by the bits WG0 and WG1
The characteristic of the peaking filter is selectable by the bits BP1 and BP0 (subaddress 01).
Even bandpass filtering can be applied. This is activated, if the BFB bit is cleared and bypass mode is set.

Details concerning the peaking functions, peaking degrees, bandpass filtering and bit addressing, are given in the VEDA data sheet.

8.1.2 CTI

Function:

The colour difference signal transients of both colour difference (U,V data) signals are shortened by a special non-linear signal processing.

The intention of the CTI function is to improve the picture display definition.

The degree of transient improvement on the U and V signal data can be chosen and thus matched to the rise and fall times of the U and V input signal data by the bits GA1, GA0 and CMO.

The DCTI gain factor is set by the bits GA1 and GA0.

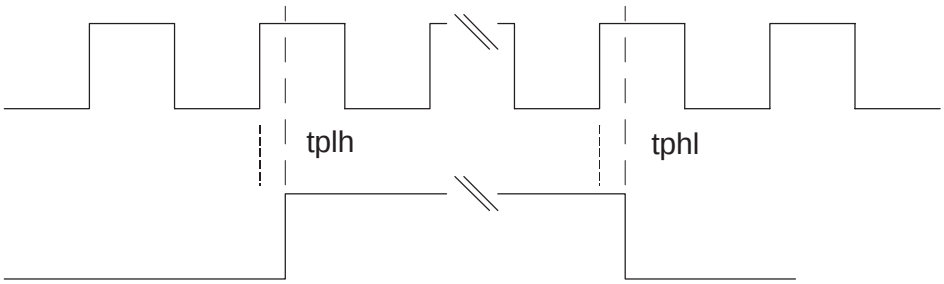
Choice modification is selectable by the CMO bit.

The U an V input signal data code is selectable, two´s complement bit DRP=0 or offset binary bit DRP=1.

Remark: The DRP bit has to be cleared in this VEDA application, see also default addressing.

9. Interface Signals IPQ Module

ST1	**Analog Output Signals**
	recommended load >= 10 KOhm
Y100	luminance signal (315mVpp), with implemented output divider, DC-coupled
-(R-Y)100	colour difference signal (1.0Vpp), 75 % saturation, DC-coupled *)
-(B-Y)100	colour difference signal (1.26Vpp), 75 % saturation, AC-coupled *)
	*): 5 % lower voltage than nom. values - compensated by higher saturation in the video processor.
ST2	**Analog Input Signals**
	nom. input level ADC 1 Vpp, inputs AC-coupled
Y50	luminance input signal (input level depends on gain setting of the preamplifier)
-(R-Y)50	colour difference input signal (1.05 Vpp), 75 % saturation
-(B-Y)50	colour difference input signal (1.33 Vpp), 75 % saturation
ST3	**Sync Input Signals**
DFLBK_I	deflection burst key input (hor. reference input for 27 MHz deflection PLL), TTL level, for not Golden Scart mode this input can be connected to ABK
SGSC_I	Switching signal for DFLK_I signal in Golden Scart mode, TTL-output
ABK	horizontal reference pulse for the acquisition PLL, TTL level, derived burst pulse from sandcastle
VACQ	vertical synchronization pulse, 50 / 60 Hz, TTL level pos.
STROBE	input signal to overrule still picture function with pixel accuracy e.g. live PIP on frozen background, TTL level.
ST4	**Supply**
	+5V 450 +/- 50 mA
	+8V 180 +/- 20 mA
ST5	**Deflection pulses and IIC-Bus**
LLDFLO	27 MHz deflection clock output (TTL level)
HDFL	hor. deflection pulse, pos. TTL
VDFL	vertical deflection pulse, pos. TTL
SCL	IIC bus clock, TTL
SDA	IIC bus data, TTL



CLK	OUT	LOAD (pF)	tplh (ns)	tphl (ns)
LLDFL	HDFL	25	12.8	15.8
LLDFL	VDFL	25	24.6	27.6

Conditions:VDD = 4.5 V;Tj = +85°C (worst case)

File: TIM_HV.WMF / 97-02-05 Ke.

Fig.6 Timing diagram for the clock relation of HDFL and VDFL

ST6 Feature Interface

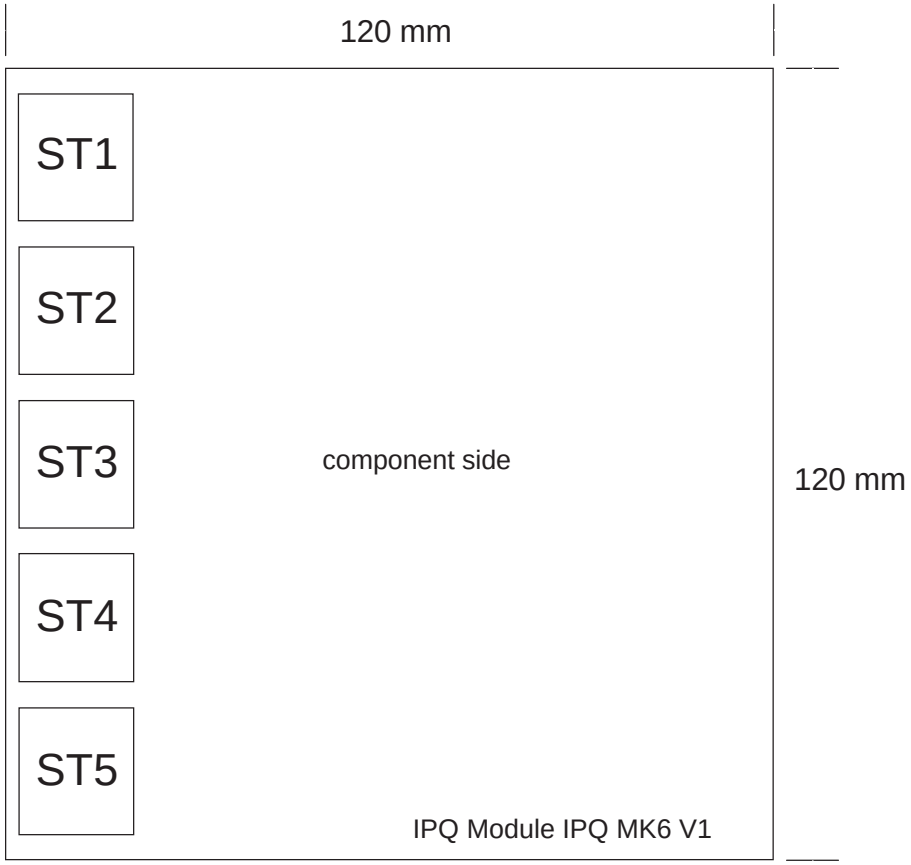
The IPQ board MK6 is equipped with a 50/60 Hz digital signal interface for add-on boards. The interface provides:

- Y and colour difference signals in the standard 4:1:1 data format,
- an acquisition clock signal,
- a write enable signal,
- a SNERT bus interface and
- + 5V supply

This interface is intended for a PALplus- or a Limeric- (SAA 4945) add-on board. If no add-on board shall be used all inputs and outputs of the interface have to be bridged by a certain bridge plug.

The PALplus application using an add-on board is decribed in the application note AN95126 [14].

10. Mechanical Outlines



File: MECHOUT.WMF / 97-03-11 Ke

Fig.7 Mechanical outlines

11. Alignment

The only components which need to be adjusted are the coils of the VCOs.

1. The IPQ Module has to be initialized. The deflection PLL is adjusted via L7. The voltage at C62 should be 3.0 V if a 15.625 KHz reference pulse (ABK) is applied to the circuit. The rising edges of the signals ABK and HRDFL are synchronized by the PLL.

2. The acquisition PLL has to be adjusted for the three possible clock frequencies. The alignment is started with the highest frequency of 18 MHz. The correct frequency mode is activated via the IIC bus (see register 1 <03>, software protocol). In this mode the coils L3 and L6 are short-circuited to achieve the highest frequency of the oscillator circuit. The frequency and phase adjustment is done with L5 in that way, that the rising edge of the signal HRA occurs in the middle of the positive ABK pulse.

In the next step the 16 MHz is adjusted by means of L6 in the same way, after a correct mode of the SAA4952 has been activated (Register 1 <02>).

Finally the lowest acquisition frequency of 13.5 MHz is aligned by means of L3, while Register 1 is set to <01>.

If PANIC is used the procedure above is reduced to the adjustment of only one acquisition frequency which equals 32 MHz. The alignment is done with L5 like described above. The coils L3 and L6 are not used and can be replaced and or short-circuit by a wire on the board.

3. The display PLL is locked to the horizontal display pulse HDFL. The adjustment is done in a way that both display frequencies 32 MHz and 36 MHz can be generated by the PLL without coil switching. The time relation between HDFL and HRD has to be checked by scope. The display frequency is switched between 32 MHz (Register 1 <0A>) and 36 MHz (Register 1 <0D>). The rising edge of HRD has to occur within the high period of HDF.

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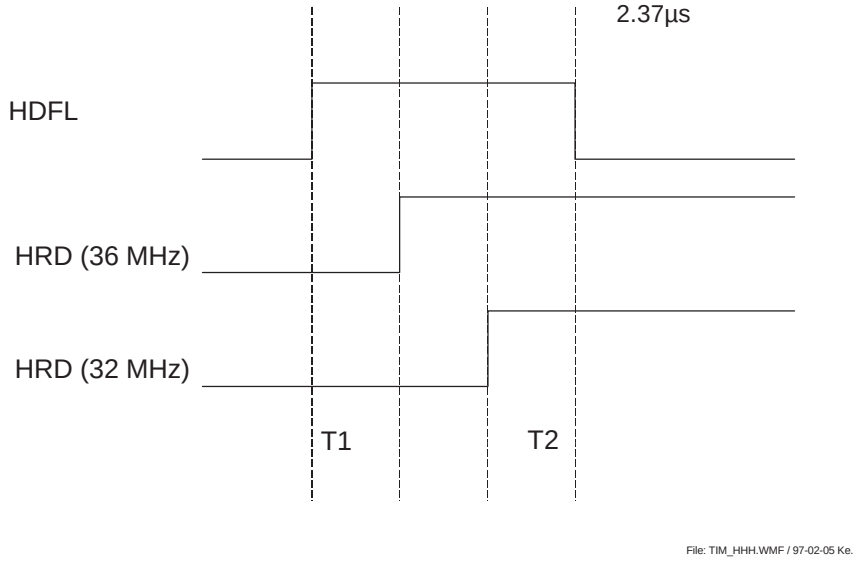

Fig.8 Time relation between HDFL and HRD (32MHz and 36MHz)

After adjustment T1 and T2 should be equal (see above).

12. Useful hints

In this chapter some hints are given how to proceed in case of malfunction of the IPQ Module.

For a proper function of the module it is fundamental that the deflection PLL is working. The 27 MHz clock is used for the parallel interface of the SAA 4952 internally, so the memory controller can only be initialized if this clock is present. The signals related to the deflection and all vertical control signals (e.g. VWE1) are processed by 27 MHz.

The u-Controller of the IPQ module is interrupted by an inverted VDFL pulse. If there are IIC-bus problems, this signal should be checked.

If mistakes occur in the picture, which seem to be related to a malfunction in the digital data path, it is useful to check the picture with LFR and noise reduction switched off. In this case only field memory 1 is active and it is easy to decide whether the mistake occurs in the feedback loop including field memory 2 or not.

In case of wrong analog signal levels at the output, the input signals of the TDA 8755 should be checked. The converter has a total range of 1 Vpp for all the three inputs (pin 3, 7, 9).

13. IPQ Module MK6 V1 circuit diagrams

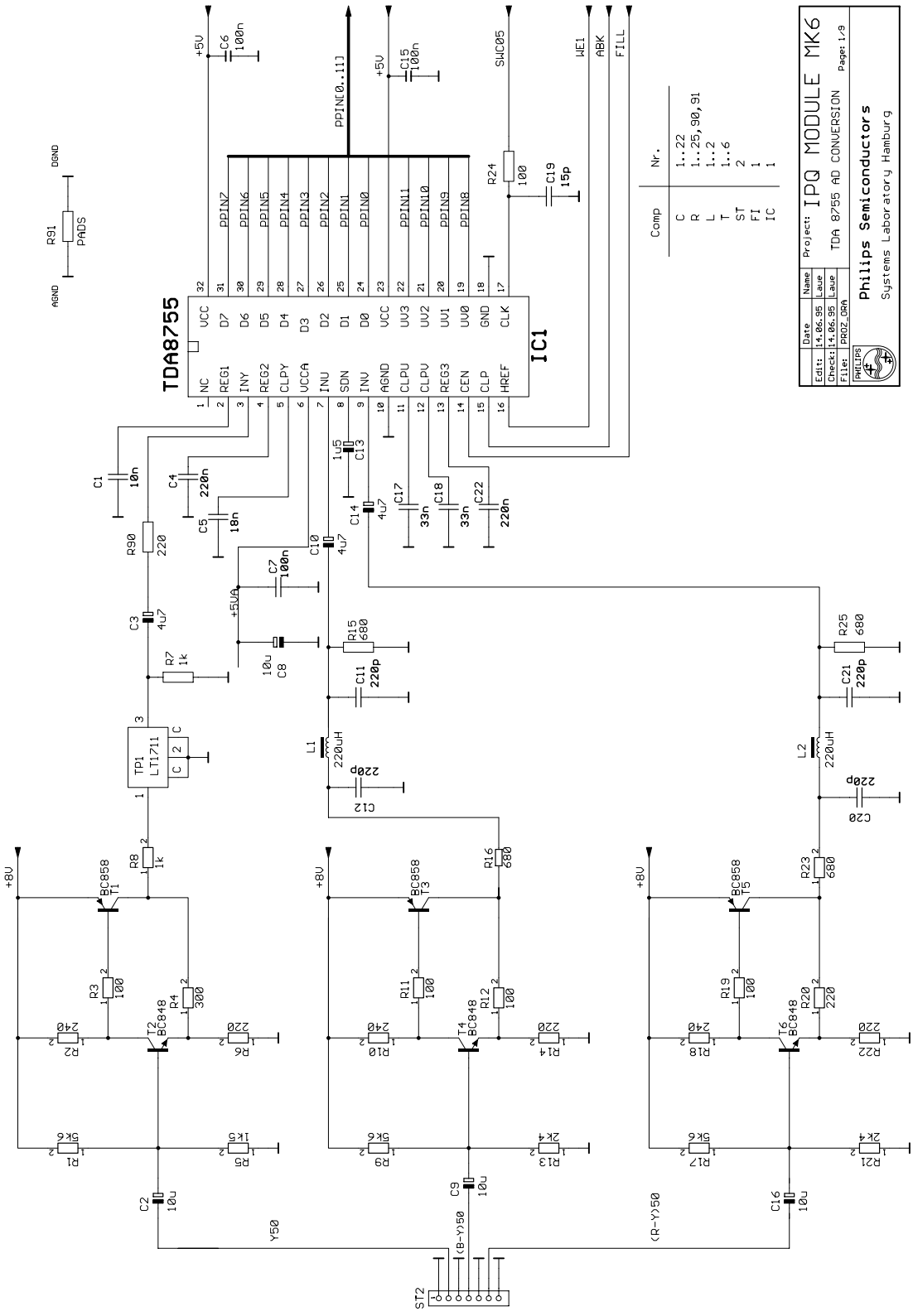

Fig.9 Circuit diagram of the AD converter

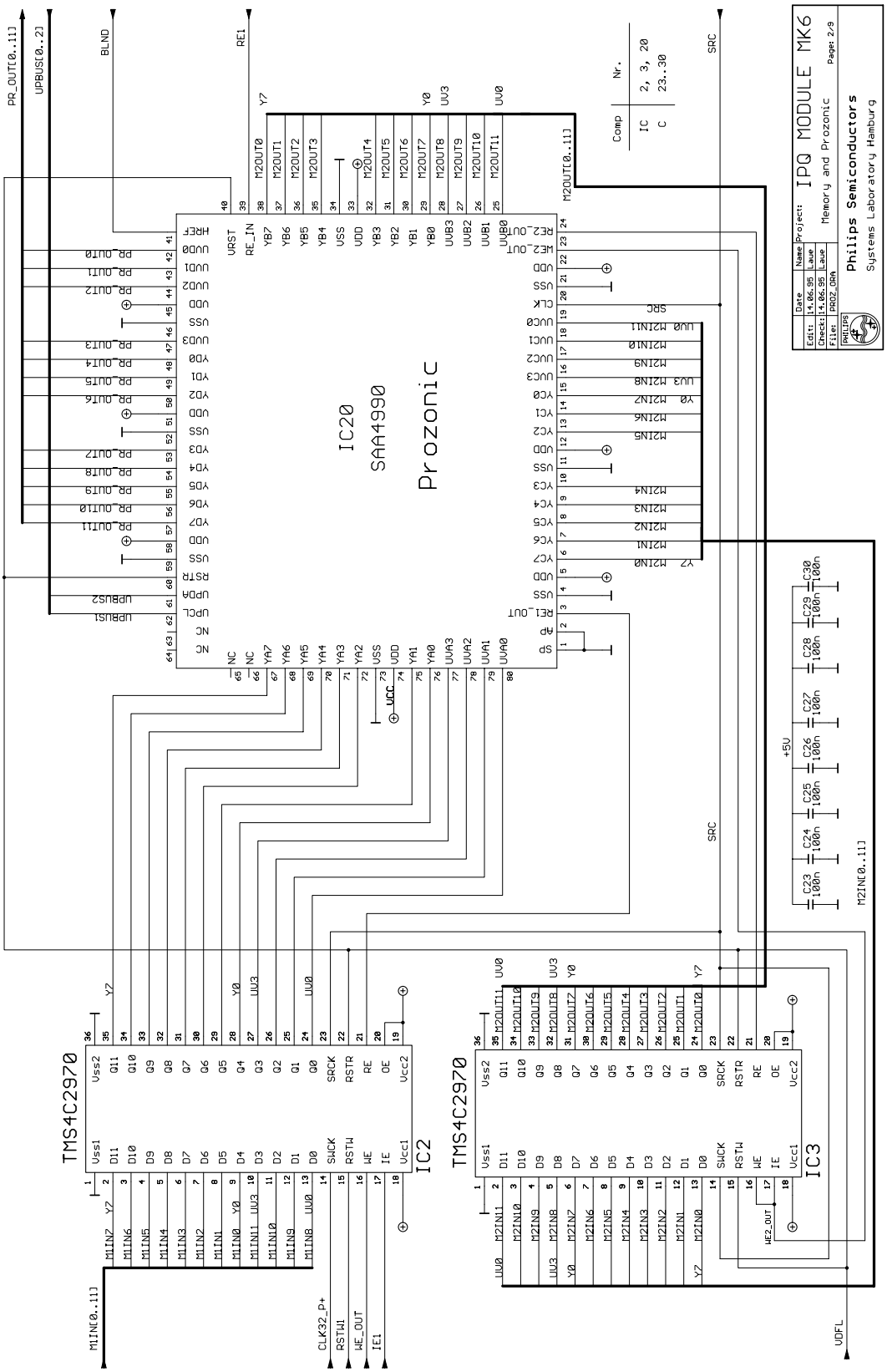

Fig.10 Circuit diagram of the memories and PROZONIC

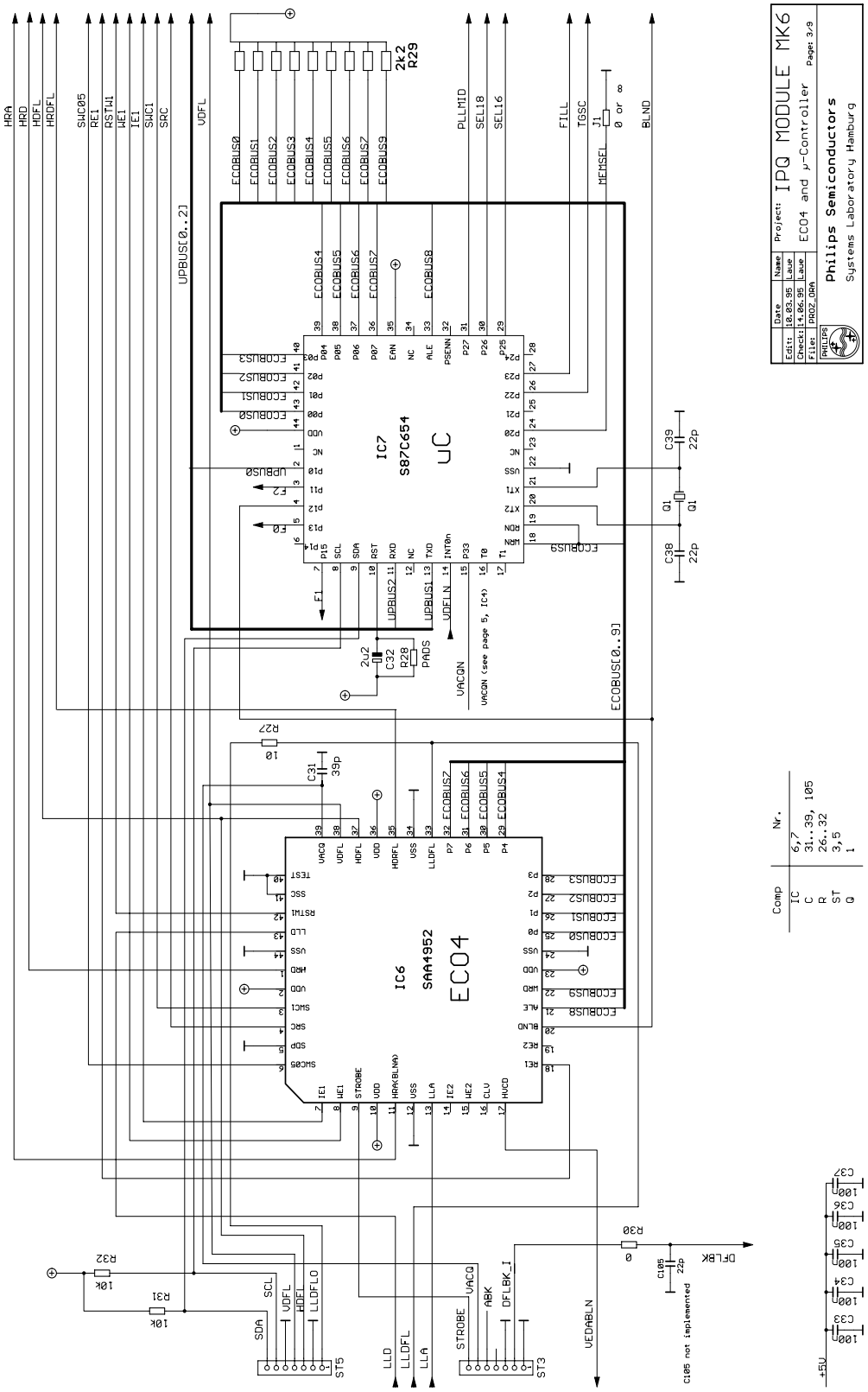

Fig.11 Circuit diagram of the ECO4 and µ-Controller

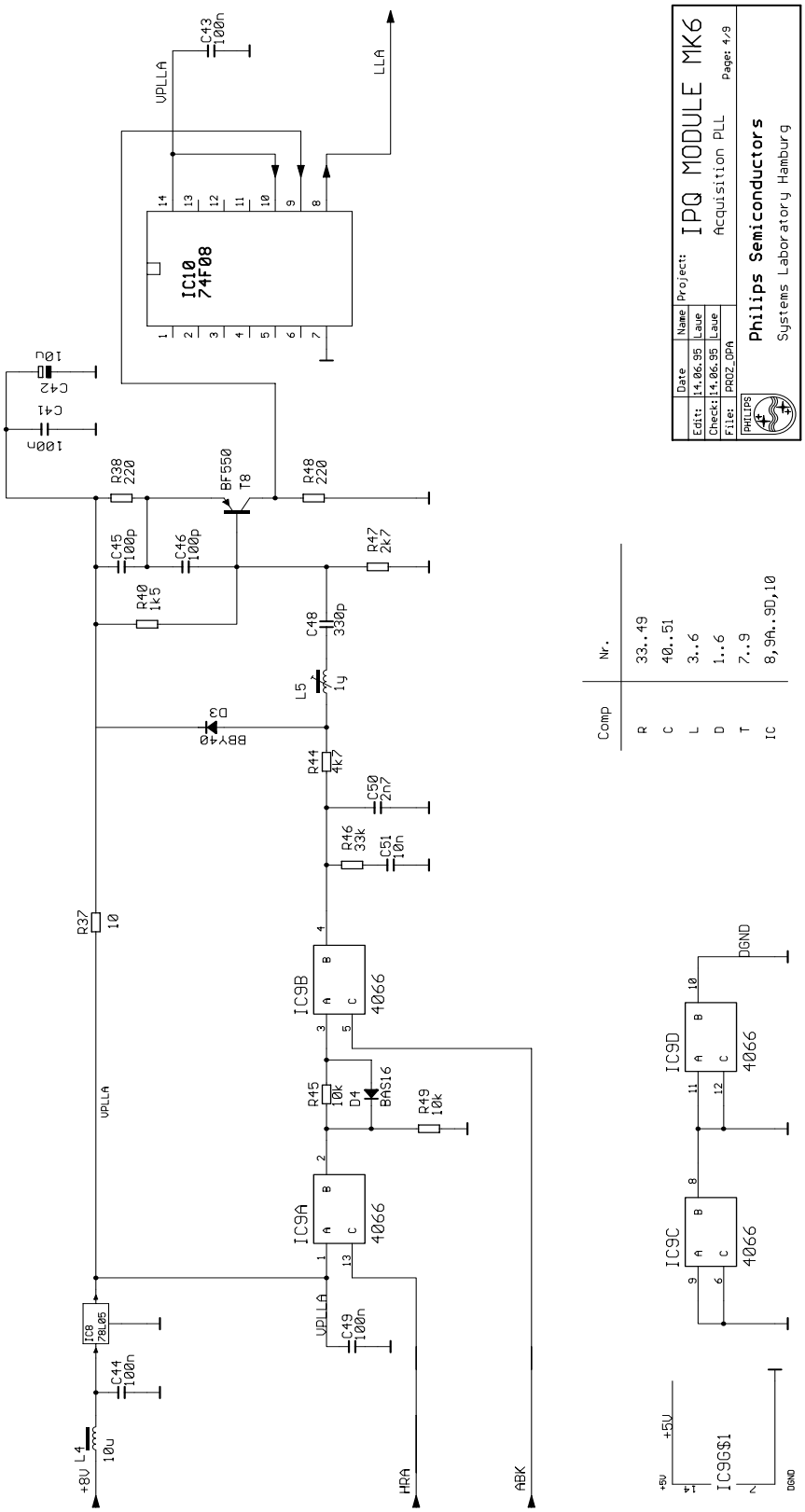

Fig.12 Circuit diagram of the Acquisition PLL

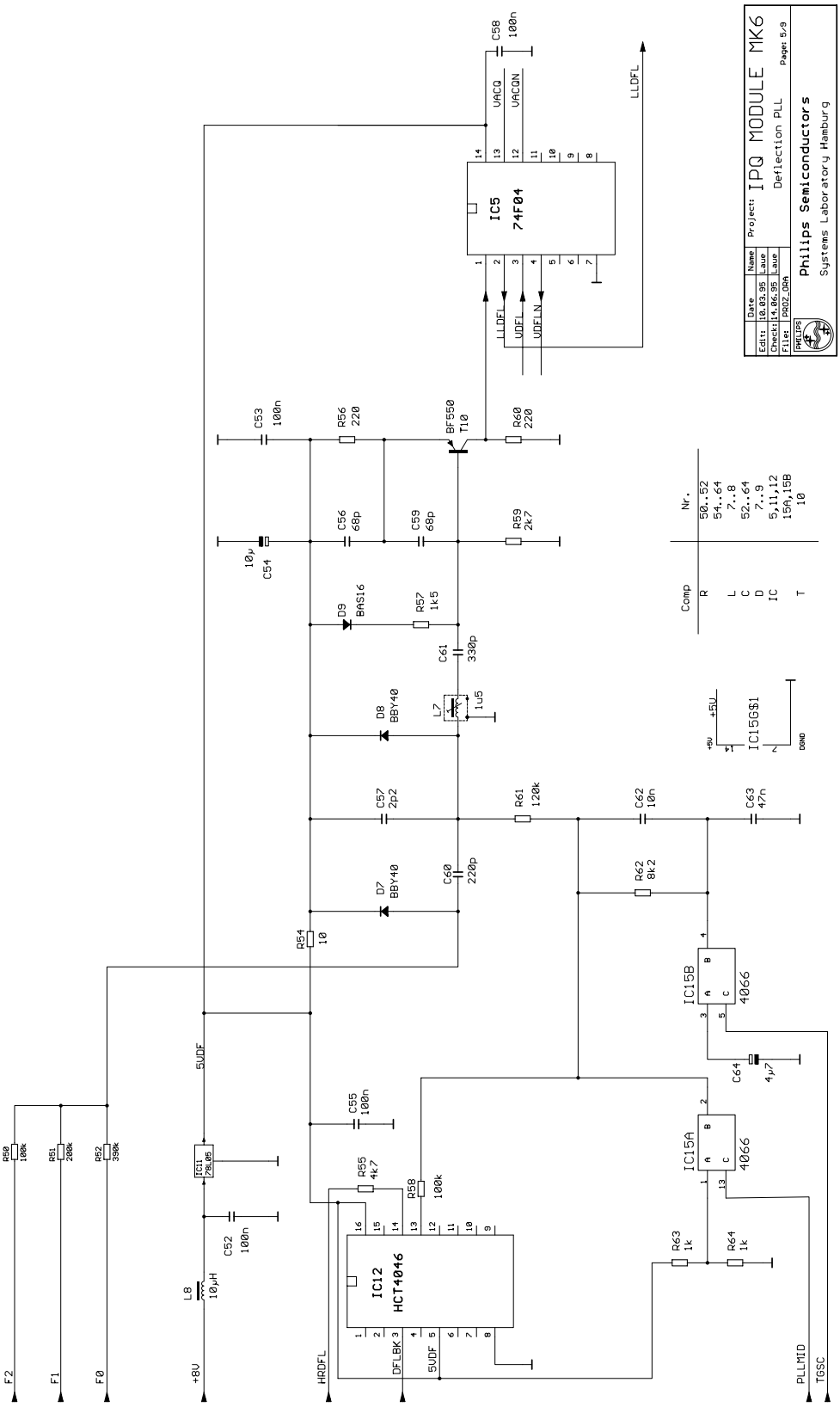

Fig.13 Circuit diagram of the Deflection PLL

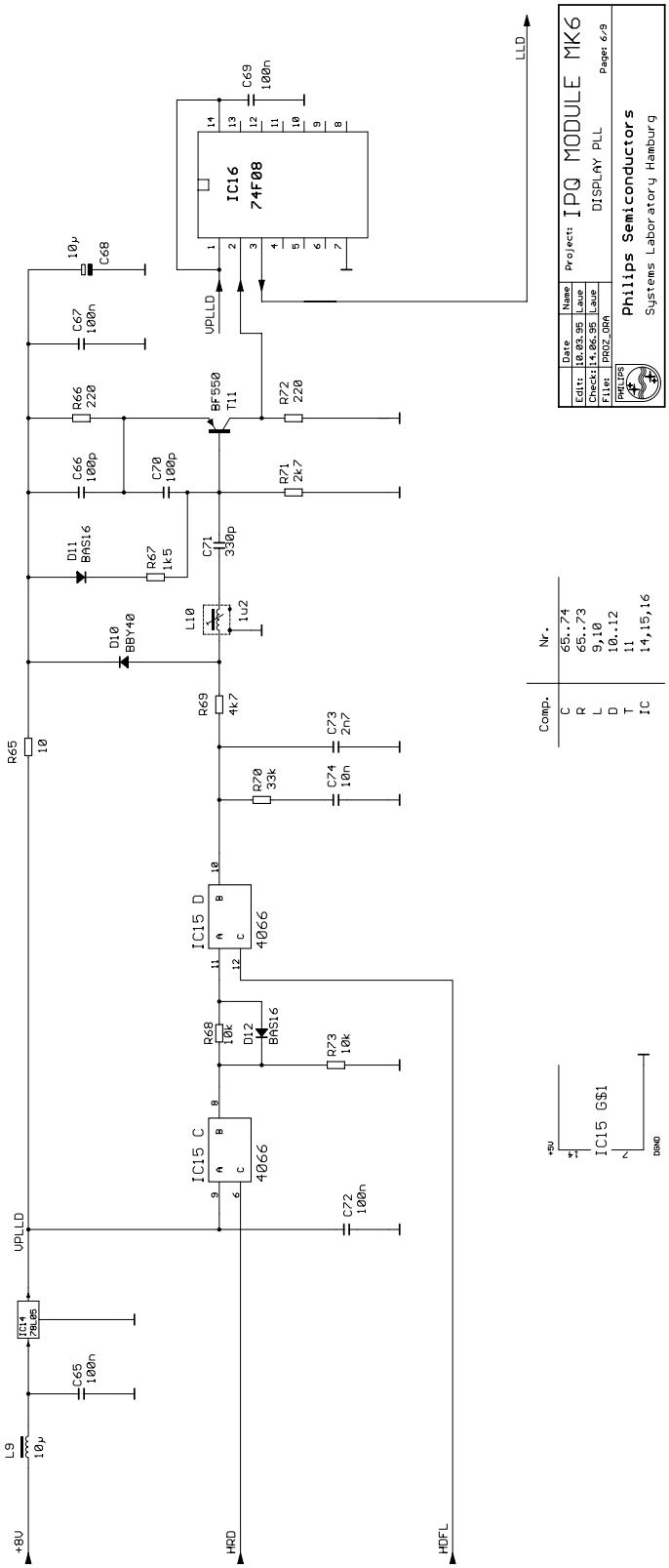

Fig.14 Circuit diagram of the Display PLL

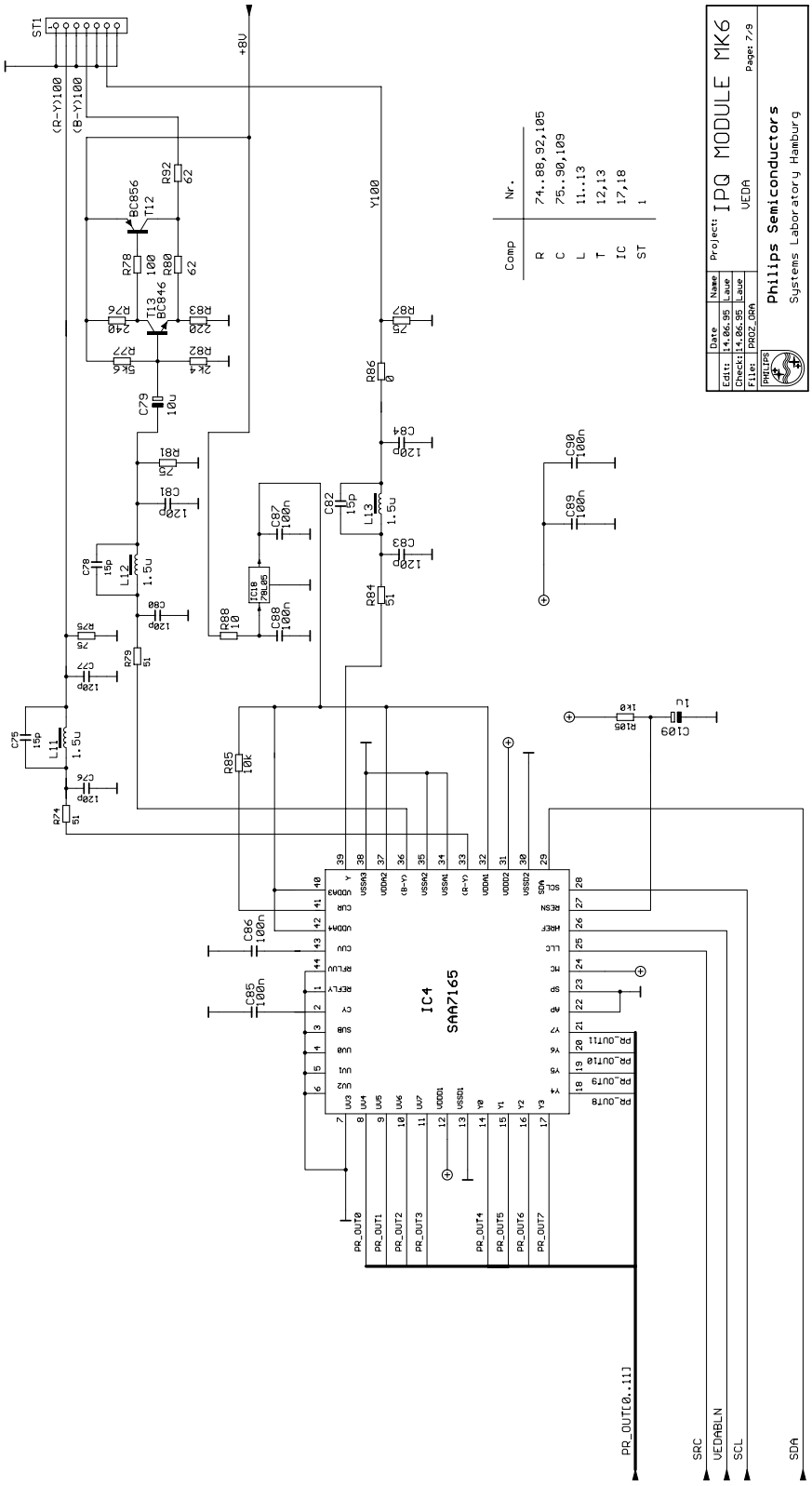

Fig.15 Circuit diagram of VEDA

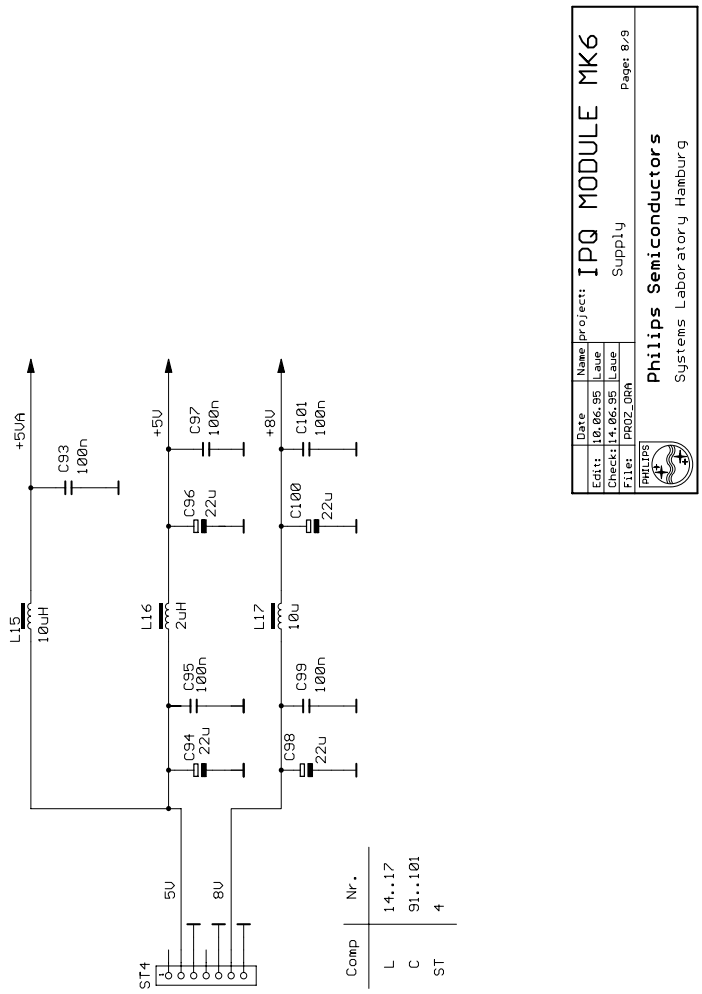

Fig.16 Circuit diagram of the supply circuit

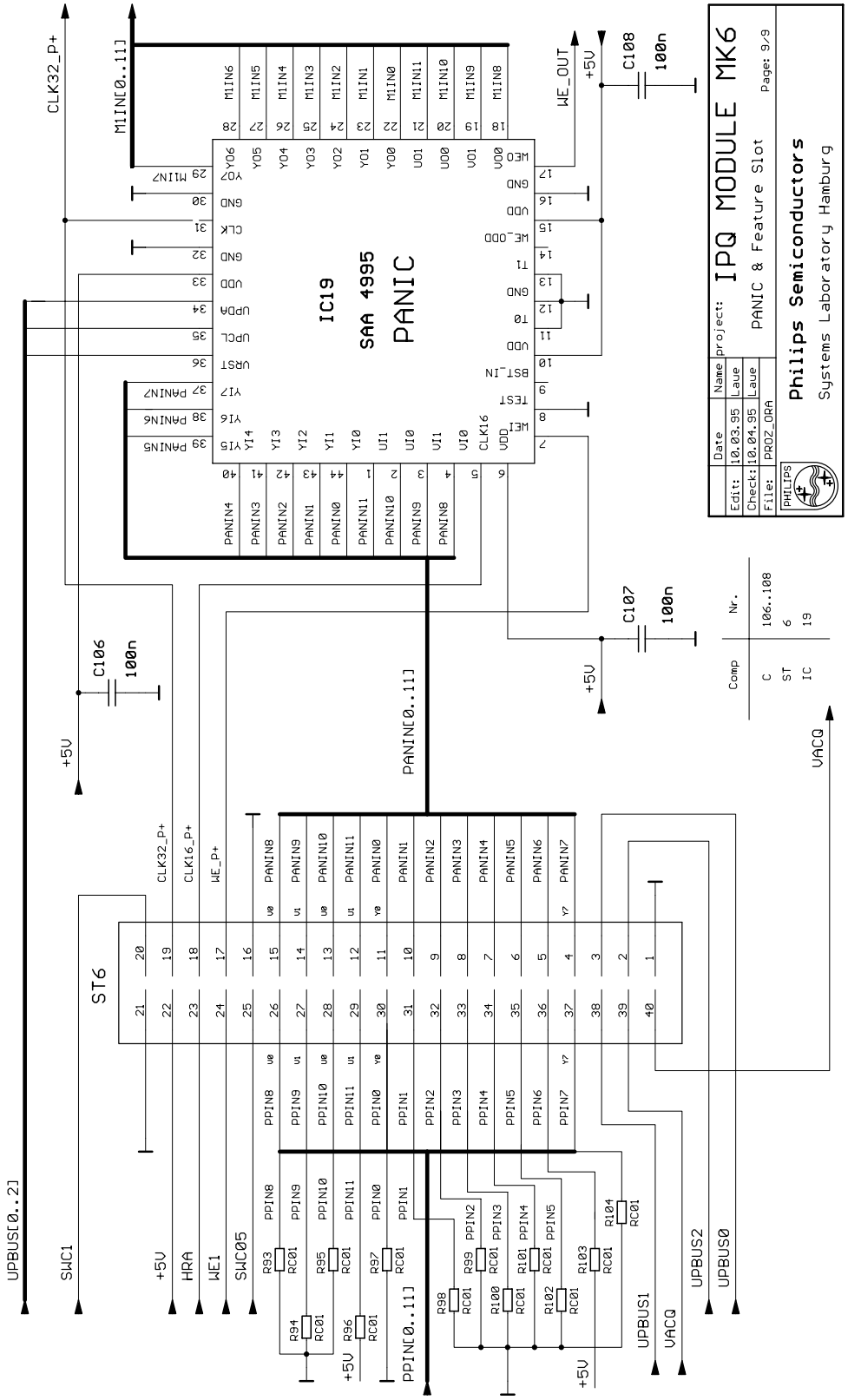

Fig.17 Circuit diagram of PANIC & Feature Slot

14. Modified circuit parts for the IPQ application without Panoramic IC

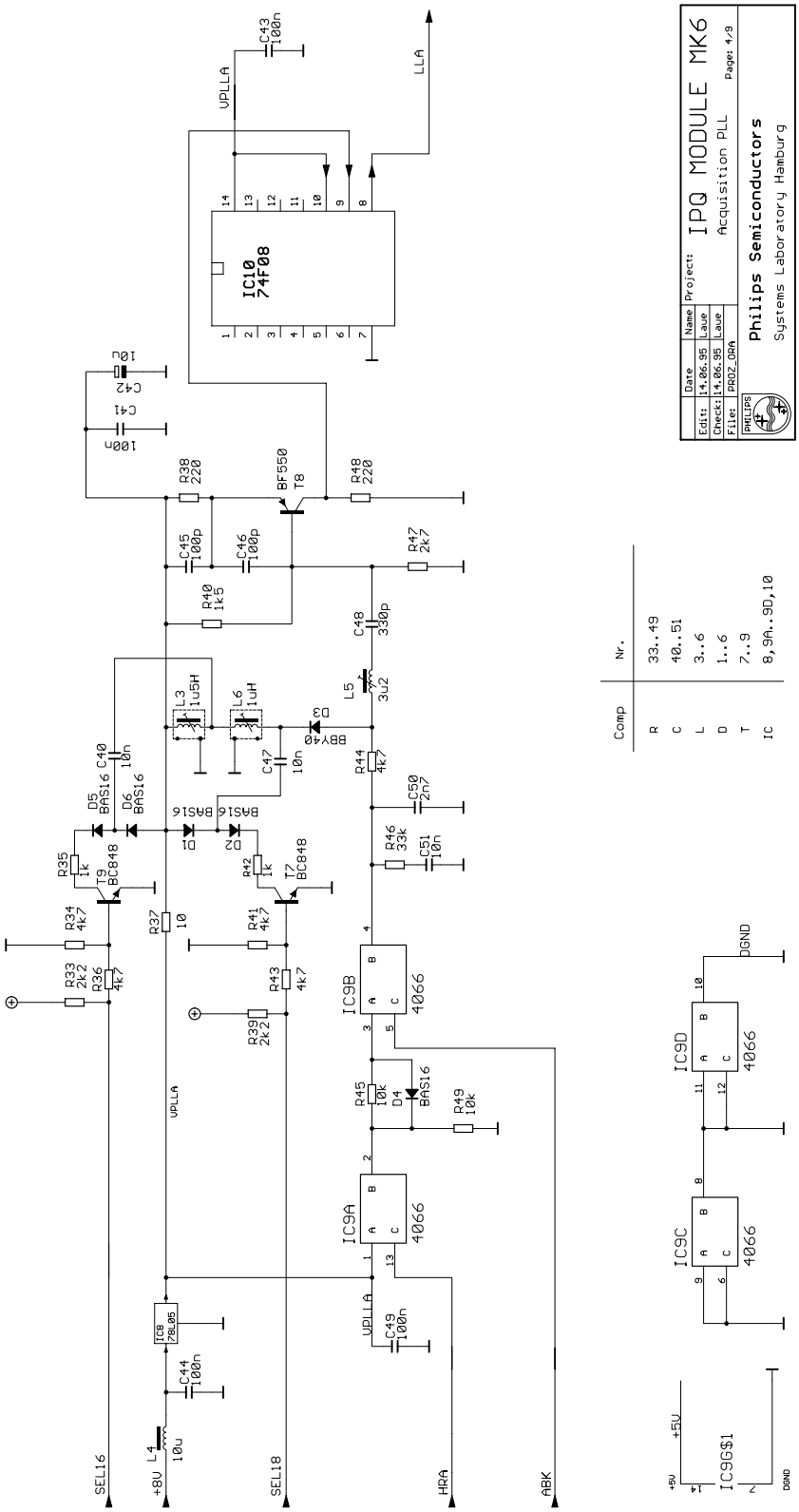

Fig.18 Circuit diagram of the Acquisition PLL, without PANIC

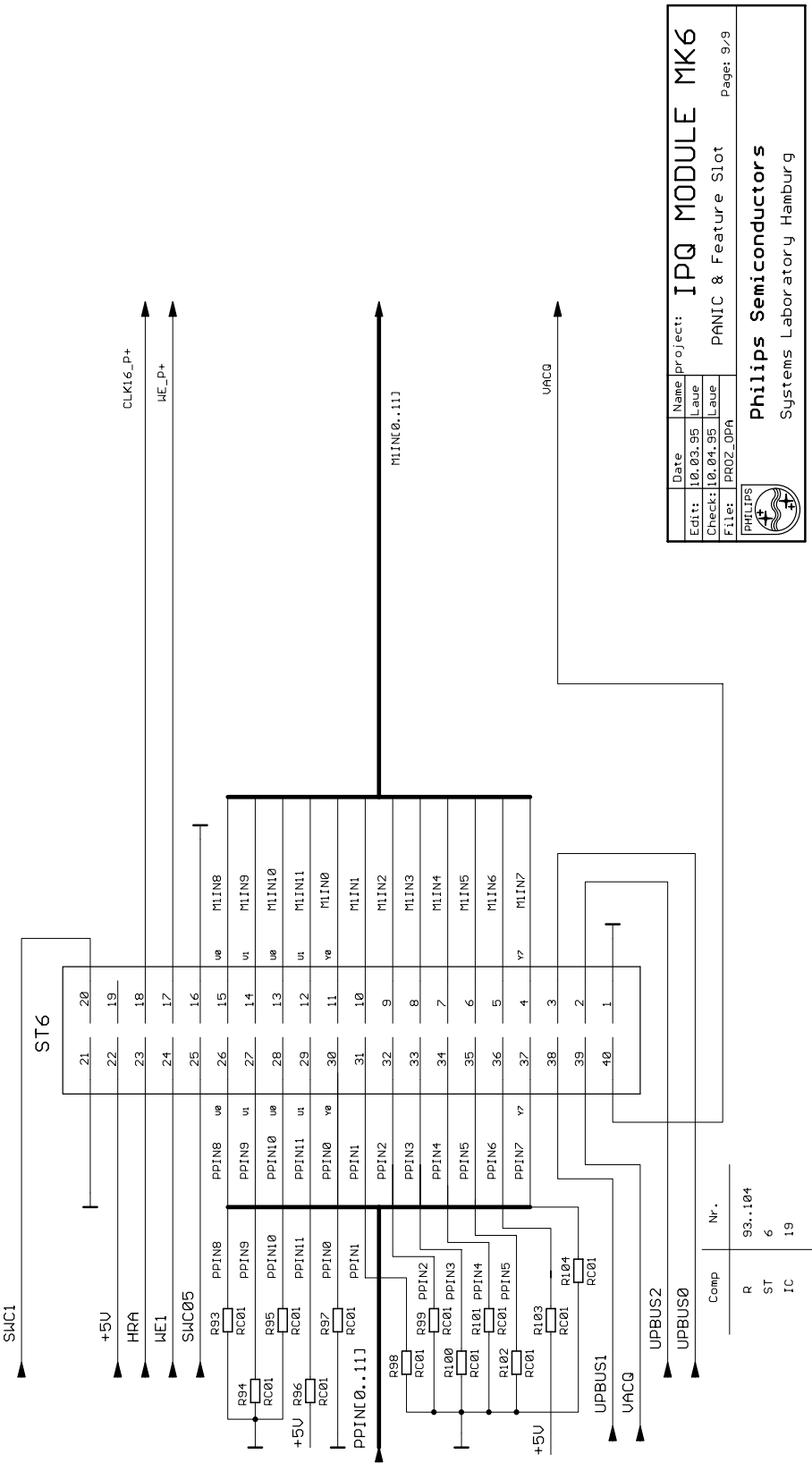

Fig.19 Circuit diagram of the Feature Slot, without PANIC

15. Assembly Plan

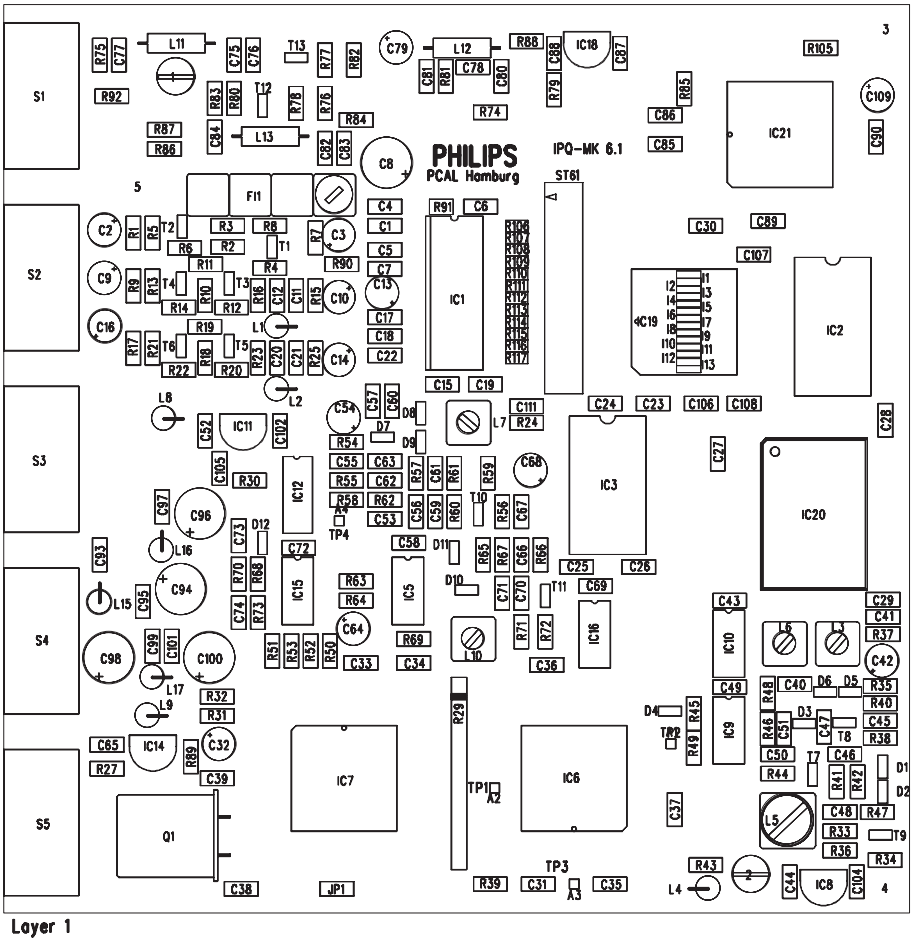

Fig.20 Top view of the completely assembled IPQ Module

16. Material list

TABLE 31 Resistors

Package	Part number	Value (Ohm)	Specification
S1206	R1	5k6	5 % tolerance, Philips RC01
	R2	240	
	R3	100	
	R4	300	1 % tolerance, Philips RC01
	R5	1k5	5 % tolerance, Philips RC01
	R6	220	1 % tolerance, Philips RC01
	R7	1k	5 % tolerance, Philips RC01
	R8	1k	
	R9	5k6	
	R10	240	
	R11	100	
	R12	100	1 % tolerance, Philips RC01
	R13	2k4	5 % tolerance, Philips RC01
	R14	220	1 % tolerance, Philips RC01
	R15	680	5 % tolerance, Philips RC01
	R16	680	
	R17	5k6	
	R18	240	
	R19	100	
	R20	220	1 % tolerance, Philips RC01
	R21	2k4	5 % tolerance, Philips RC01
	R22	220	1 % tolerance, Philips RC01
	R23	680	5 % tolerance, Philips RC01
	R24	100	
	R25	680	
	R26	0	Philips RC01
	R27	10	5 % tolerance, Philips RC01
SIP10	R29	2k2	resistor array, 9 x 2k2

TABLE 31 Resistors

Package	Part number	Value (Ohm)	Specification
S1206	R30	0	Philips RC01
	R31	10k	5 % tolerance, Philips RC01
	R32	10k	
	R33 *)	2k2	
	R34 *)	4k7	
	R35 *)	1k	
	R36 *)	4k7	
	R37	10	
	R38	100 or 220 #)	
	R39 *)	2k2	
	R40	1k5	
	R41 *)	4k7	
	R42 *)	1k	
	R43 *)	4k7	
	R44	4k7	
	R45	10k	
	R46	33k	
	R47	2k7	
	R48	220	
	R49	10k	
	R50	100k	
	R51	100k	
	R52	100k	
	R54	4k7	
	R55	4k7	
	R56	not impl	
	R57	1k5	
	R58	100k	

TABLE 31 Resistors

Package	Part number	Value (Ohm)	Specification
S1206	R59	2k7	5 % tolerance, Philips RC01
	R60	220	
	R61	120k	
	R62	8k2	
	R63	1k	
	R64	1k	
	R65	10	
	R66	150 or 220 #)	
	R67	1k5	
	R68	10k	
	R69	4k7	
	R70	33k	
	R71	2k7	
	R72	220	
	R73	10k	
	R74	51	
	R75	75	
	R76	240	
	R77	5k6	
	R78	100	
	R79	51	
	R80	62	1 % tolerance
	R81	75	5 % tolerance, Philips RC01
	R82	2k4	
	R83	220	1 % tolerance
	R84	51	5 % tolerance, Philips RC01
	R85	10k	
	R86	0	Philips RC01
	R87	75	5 % tolerance, Philips RC01

TABLE 31 Resistors

Package	Part number	Value (Ohm)	Specification
S1206	R88	10	5 % tolerance, Philips RC01
	R90	220	
	R91	62	
	R92	62	
	R93	47K	
	R94	47K	
	R95	47K	
	R96	47K	
	R97	47K	
	R98	47K	
	R99	47K	
	R100	47K	
	R101	47K	
	R102	47K	
	R102	47K	
	R103	47K	
	R104	47K	
	R105	1k	

TABLE 32 Capacitors

Package	Part number	Value (Farad)	Specification
S1206	C1	10n	Philips Standard Series X7R
Pin spacing: 2.54 mm	C2	10µ	Philips electrolytic capacitor RLP 5-134, 16V, 25V radial
	C3	4µ7	
S1206	C4	220n	Philips Standard Series X7R
	C5	220n	
	C6	100n	
	C7	100n	
Pin spacing: 5.08 mm	C8	10µ	Standard El. Capacitor 16V, radial
Pin spacing: 2.54 mm	C9	10µ	Philips electrolytic capacitor RLP 5-134, 16V, 25V radial
	C10	4µ7	
S1206	C11	220p	Philips Standard Series X7R
	C12	220p	
Pin spacing: 2.54 mm	C13	1µ5	Philips Tantalum 16V radial Philips electrolytic capacitor RLP 5-134, 16V radial
	C14	4µ7	
S1206	C15	100n	Philips Standard Series X7R
Pin spacing: 2.54 mm	C16	10µ	Philips electrolytic capacitor RLP 5-134, 16V radial
S1206	C17	33n	Philips Standard Series X7R
	C18	33n	
	C19	15p	
	C20	220p	
	C21	220p	
	C22	220n	
	C23	100n	
	C24	100n	
	C25	100n	
	C26	100n	
	C27	100n	

TABLE 32 Capacitors

Package	Part number	Value (Farad)	Specification
S1206	C28	100n	Philips Standard Series X7R
	C29	100n	
	C30	100n	
	C31	39p	
Pin spacing: 2.54 mm	C32	2µ2	Philips electrolytic capacitor RLP 5-134, 35V radial
S1206	C33	100n	Philips Standard Series X7R
	C34	100n	
	C35	100n	
	C36	100n	
	C37	100n	
	C38	22p	
	C39	22p	
	C40 *)	10n	
	C41	100n	
Pin spacing: 2.54 mm	C42	10µ	Philips electrolytic capacitor RLP 5-134,16V radial
S1206	C43	100n	Philips Standard Series X7R
	C44	100n	
	C45	220p	
	C46	220p	
	C47 *)	10n	
	C48	330p	
	C49	100n	
	C50	2n7	
	C51	10n	
	C52	100n	
	C53	100n	
Pin spacing: 2.54 mm	C54	10µ	Philips electrolytic capacitor RLP 5-134,16V radial

TABLE 32 Capacitors

Package	Part number	Value (Farad)	Specification
S1206	C55	100n	Philips Standard Series X7R
	C56	68p	
	C57	27p	
	C58	100n	
	C59	68p	
	C60	220p	
	C61	330p	
	C62	10n	
	C63	47n	
Pin spacing: 2.54 mm	C64	4u7F	Philips electrolytic capacitor RLP 5-134, 25V radial
S1206	C65	100n	Philips Standard Series X7R
	C66	100p	
	C67	100n	
Pin spacing: 2.54 mm	C68	10µ	Philips electrolytic capacitor RLP 5-134, 25V radial
S1206	C69	100n	Philips Standard Series X7R
	C70	100p	
	C71	330p	
	C72	100n	
	C73	2n7	
	C74	10n	
	C75	15p	
	C76	120p	
	C77	120p	
	C78	15p	
Pin spacing: 2.54 mm	C79	10µ	Philips electrolytic capacitor RLP 5-134,16V radial

TABLE 32 Capacitors

Package	Part number	Value (Farad)	Specification
S1206	C80	120p	Philips Standard Series X7R
	C81	120p	
	C82	15p	
	C83	120p	
	C84	120p	
	C85	100n	
	C86	100n	
	C87	100n	
	C88	100n	
	C89	100n	
	C90	100n	
Pin spacing: 5.08 mm	C91	not impl.	
S1206	C92	not impl.	Philips Standard Series X7R
	C93	100n	
Pin spacing: 5.08 mm	C94	22µ	Standard El. Capacitor 16V, radial
S1206	C95	100n	Philips Standard Series X7R
Pin spacing: 5.08 mm	C96	22µ	Standard El. Capacitor 16V, radial
S1206	C97	100n	Philips Standard Series X7R
Pin spacing: 5.08 mm	C98	22µ	Standard El. Capacitor 16V, radial
S1206	C99	100n	Philips Standard Series X7R
Pin spacing: 5.08 mm	C100	22µ	Standard El. Capacitor 16V, radial
S1206	C101	100n	Philips Standard Series X7R
S1206	C105	22p.	
S1206	C106 *)	100n	
S1206	C107 *)	100n	
S1206	C108 *)	100n	

TABLE 33 ICs

Package	Part number	Device	Specification
SOL32	IC1	TDA8755T	Triple ADC, Philips CAEN
SSOP36	IC2	TMS4C2970-26DT	Field memories, Texas Instruments
	IC3	TMS4C2970-26DT	
SO14	IC5	N74F04D	Hex Inverter, Philips Semiconductors
PLCC44	IC6	SAA4952WP	ECO4 Memory Controller, Philips Semiconductors
PLCC44 on socket	IC7	P83C654FBA ROM version or S87C654-4A44 EPROM version	8 bit Microcontroller, Philips Semiconductors (should be implemented on surface mount PLCC socket, pads of socket and IC identical) PCS-044SMU-11, AUGAT)
TO-92	IC8	78L05ACP	Voltage Regulator
SO14	IC9	74HCT4066T	Quad bilateral switches
SO14	IC10	74F08D	Quad AND gates
TO-92	IC11	78L05ACP	Voltage Regulator
SO16	IC12	74HCT4046AT	Digital Phase comparator
TO-92	IC14	78L05ACP	Voltage Regulator
SO14	IC15	74HCT4066T	Quad bilateral switches
SO14	IC16	74F08D	Quad AND gates
QFP80	IC 20	SAA4990	PROZONIC, Philips Semiconductors
TO-92	IC18	78L05ACP	Voltage Regulator
PLCC44	IC19 #)	SAA4995WP	PANIC, Philips Semiconductors, #)optional
PLCC	IC21	SAA716WP	VEDA, Philips Semiconductors

TABLE 34 Discrete Semiconductors

Package	Part number	Device	Specification
SOT23	D1 *)	BAS16	Diode, Philips Semiconductors
	D2 *)		
	D3	BBY40	Cap. Diode, Philips Semiconductors
	D4	BAS16	Diode, Philips Semiconductors
	D5 *)		
	D6 *)		
	D7	BBY40	Cap .Diode, Philips Semiconductors
	D8	BBY40	Cap .Diode, Philips Semiconductors
	D9	BAS16	Diode, Philips Semiconductors
	D10	BBY40	Cap. Diode, Philips Semiconductors
	D11	BAS16	Diode, Philips Semiconductors
	D12		
	T1	BC858	PNP Transistor, Philips Semiconductors
	T2	BC848	NPN Transistor, Philips Semiconductors
	T3	BC858	PNP Transistor, Philips Semiconductors
	T4	BC848	NPN Transistor, Philips Semiconductors
	T5	BC858	PNP Transistor, Philips Semiconductors
	T6	BC848	NPN Transistor, Philips Semiconductors
	T7 *)	BC848	NPN Transistor, Philips Semiconductors
	T8	BF550	PNP HF-Transistor, Philips Semiconductors
	T9 *)	BC848	NPN Transistor, Philips Semiconductors
	T10	BF550	PNP HF-Transistor, Philips Semiconductors
	T11	BF550	PNP HF-Transistor, Philips Semiconductors
	T12	BC858	PNP Transistor, Philips Semiconductors
	T13	BC848	NPN Transistor, Philips Semiconductors

TABLE 35 Coils and Filters

Package	Part number	Device	Value (Henry)	Specification
	L1		220µ	Fixed Coil, axial, Prefilter
	L2			
	L3 *)	638AN-0166Z	1µ5	5CCE, TOKO Coil, PLL alignment
	L4		10µ	Fixed Coil, axial, RF suppressor coil
	L5	7KN 113CN2K843	3u2 or 1µ#)	TOKO Coil, PLL alignment, #) for PANIC appl.
	L6 *)	638AN-0164Z	1u0	5CCE, TOKO coil, PLL alignment
	L7	638AN-0166Z	1u5	
	L8		10µ	Fixed Coil, axial, RF suppressor coil
	L9			
	L10	638AN-0165Z	1µ2	5CCE, TOKO coil, PLL alignment
	L11		1µ5	Fixed Coil, axial, Postfilter
	L12			
	L13			
	L14		10µ	Fixed Coil, axial, RF suppressor coil
	L15			
	L16		2µ	Ferrit, RF suppressor coil, axial
	L17		10µ	Fixed coil, axial, RF suppressor coil
	FI1	5VFQ; H316LSN-1711QCD	5.5 MHz cutoff freq.	Lowpass Antialiasingfilter, Blockfilter

TABLE 36 Crystal

Package	Part number	Value (MHz)	Specification
RW-43 Metal case	Q1	12	Parallel resonance operation

TABLE 37 Connectors

Package	Part number	Specification
7 pins, pin spacing 2.5mm	ST1	Stocko-Connector MKF 1507-1-0-707
	ST2	
	ST3	
	ST4	
	ST5	

Remarks:

*) These components can be removed in case of PANIC application.
#) Suitable components value for PANIC application.

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